



Project Name

Application Note #016 (AN016-V1.1)

AN

[MiDAS1.x/MiDAS2.x] Characteristics of CORERIVER's ADC

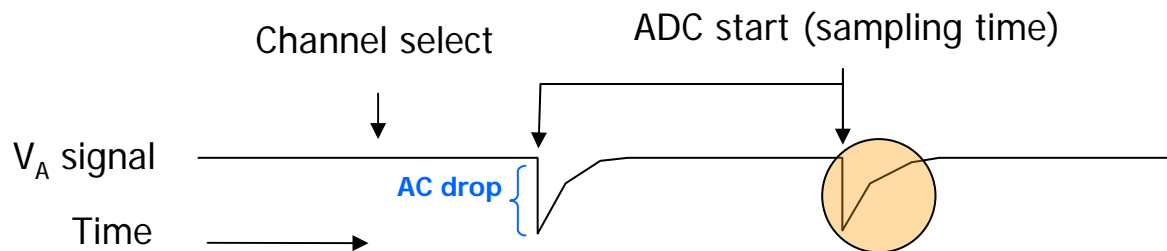
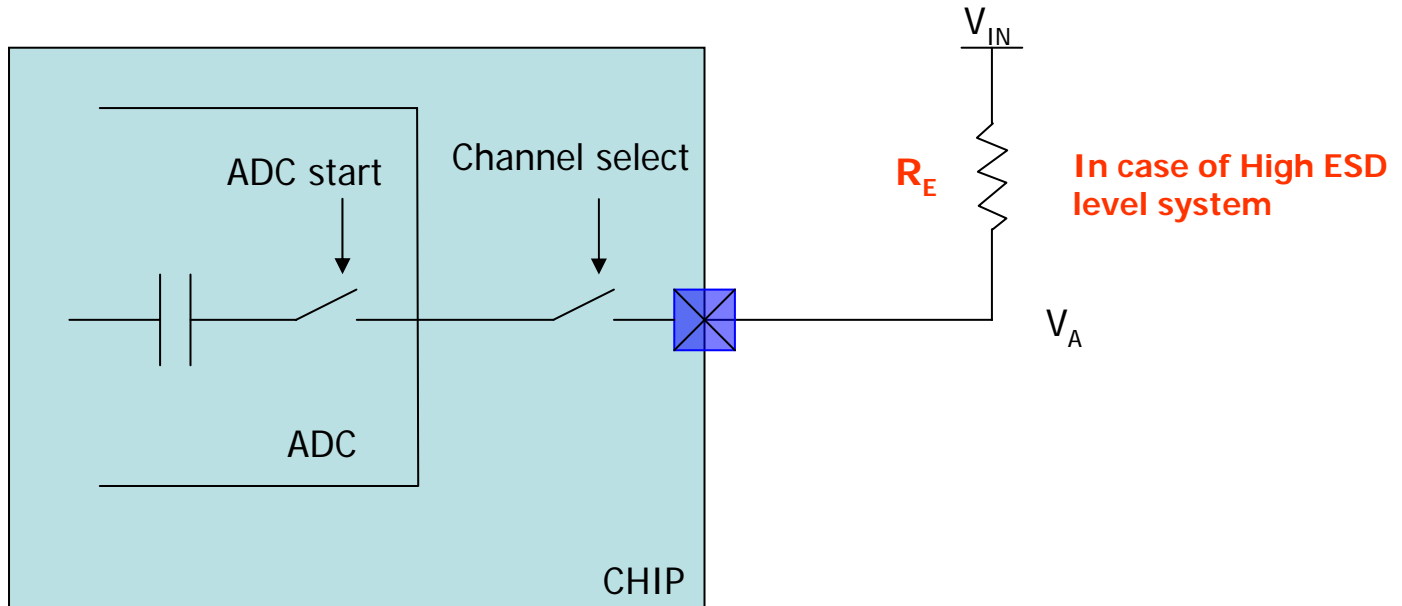
In case of a series resistor at the input channel

V1.1

October 2006

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1. Input stage of ADC and it's results



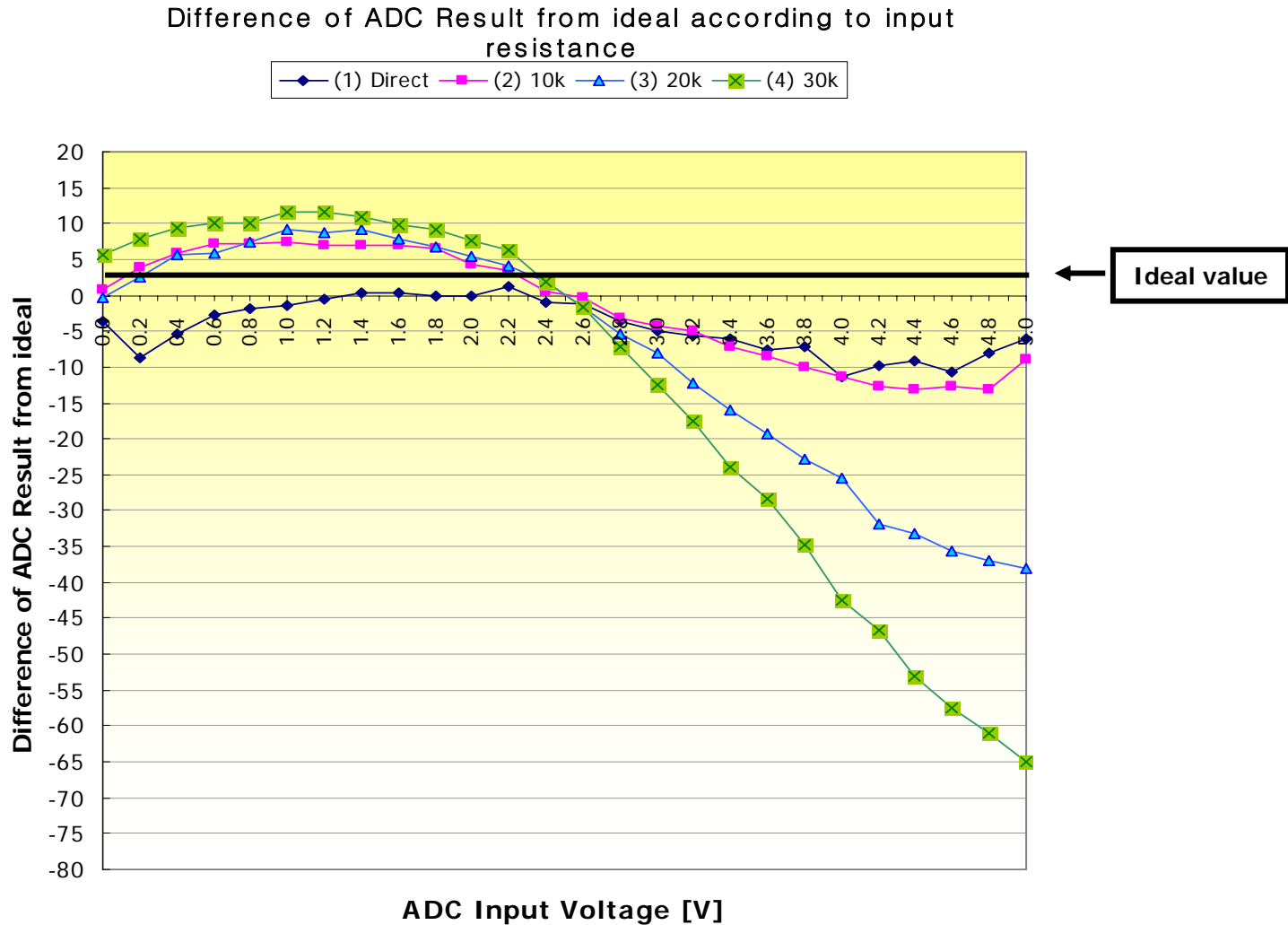
AC drop : When ADC start signal is enabled, V_A node is dropped abruptly because of a internal resistors and capacitors.

Its state will be recovered in a short time

Sampling time : That moment, if the sampling is done early, the output will not have a right value.

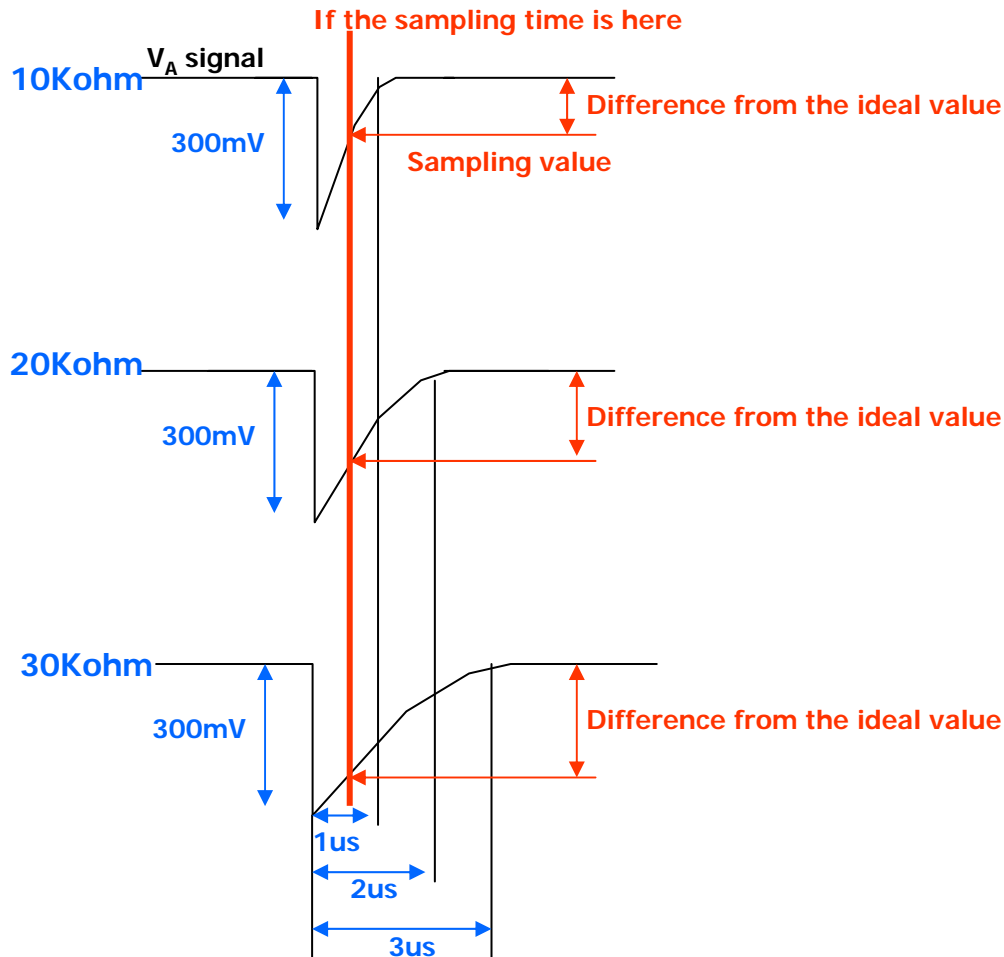
2. ADC output value by the series resistor

◆ ADC output values by the series resistance

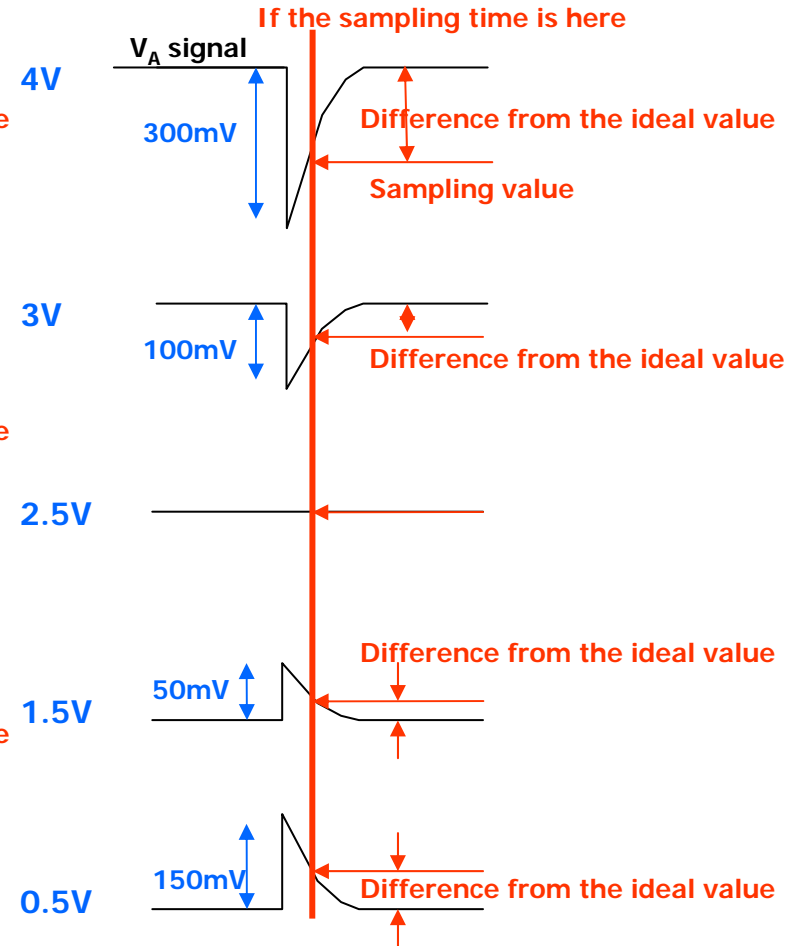


2.1. Experiments and Analysis

- ◆ Difference of ADC input value by the series resistance (@ $A_{IN} = 4V$)



- ◆ Difference of ADC input value by the input voltage (@ $R_E = 30Kohm$)

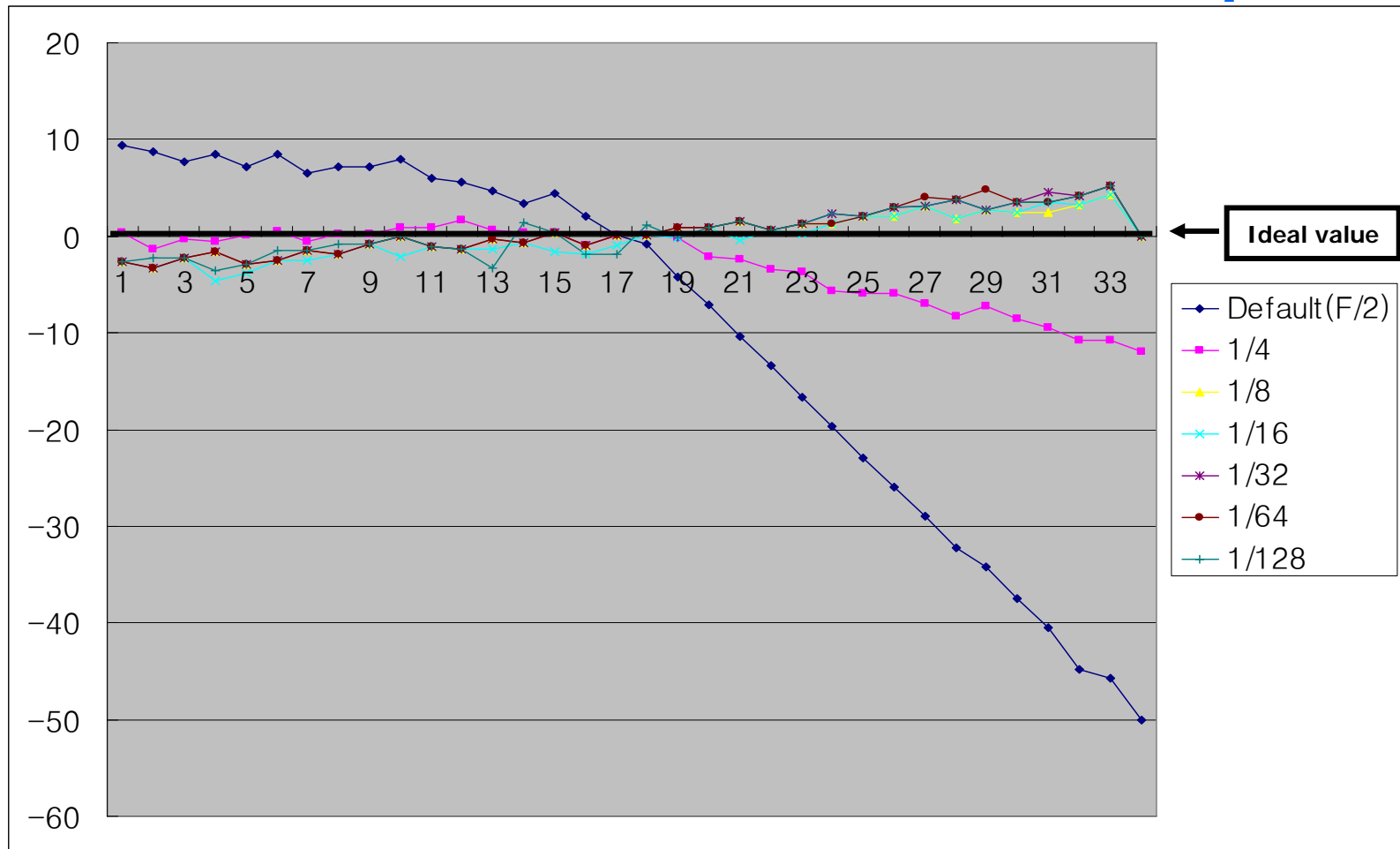


3. ADC output value by ADC sampling frequency

◆ Difference ADC output value according to ADC sampling frequency ($F=11\text{MHz}$)

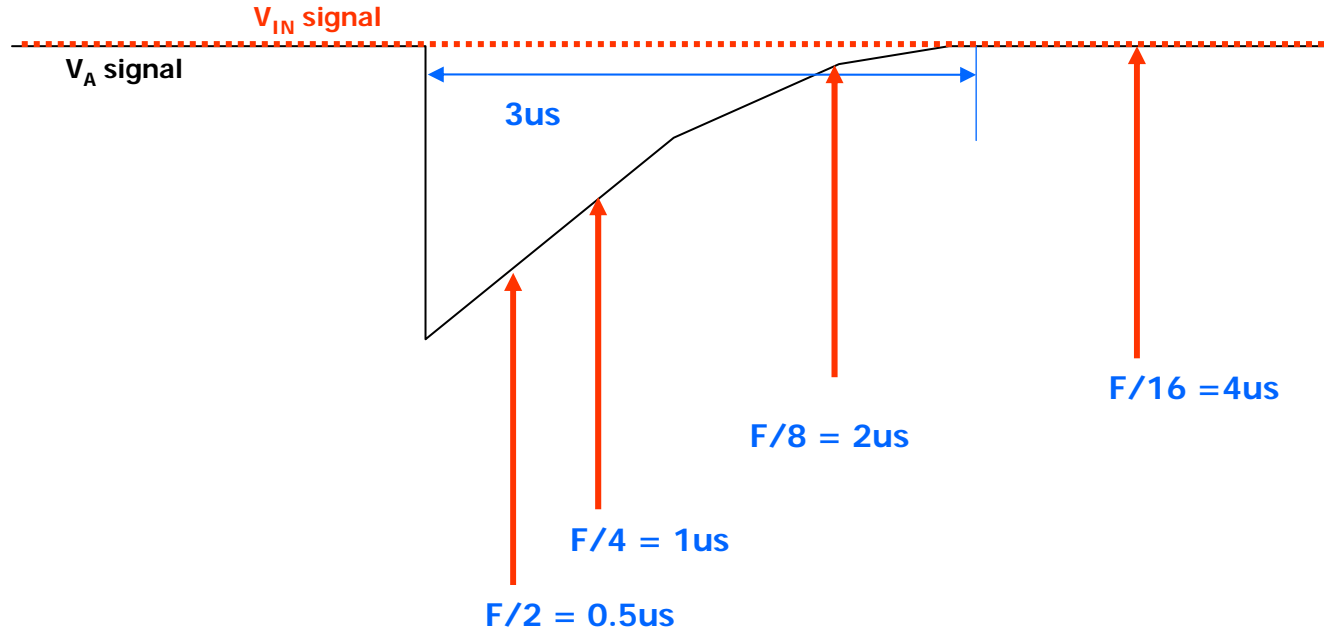
✓ Divide ratio is over $(1/8)F$, output value is almost same to the ideal value

$R_E = 30\text{Kohm}$



3-1. Experiments and Analysis

- ◆ ADC sampling point by ADC sampling time



- ✓ If it is a higher divide ratio, the sampling point is closer to the input signal (V_{IN}).
- ✓ Over the divide ratio of $F/8$, the results is almost same.
- ✓ lower Frequency, better result.
- ✓ lower resistor, better result.

3-2. Relationship of resistance and frequency

◆ Relationship of the series resistance and the sampling frequency

If, $R_E=10K\Omega$, then, recovery time = 1us, By design, sampling clock = 5, that is, 1period = 200ns $\rightarrow F_{ADC}=5MHz$

$R_E=20K\Omega$, recovery time = 2us, sampling clock = 5, 1clock = 400ns, $F_{ADC}=2.5MHz$

$R_E=30K\Omega$, recovery time = 3us, sampling clock = 5, 1clock = 600ns, $F_{ADC}=1.6MHz$

R_E and F_{ADC} are in inverse proportion,

We can establish a new relationship of $F_{ADC} = A \times (1/R_E)$,

Where, $A = 50 \times 10^9$

That is,

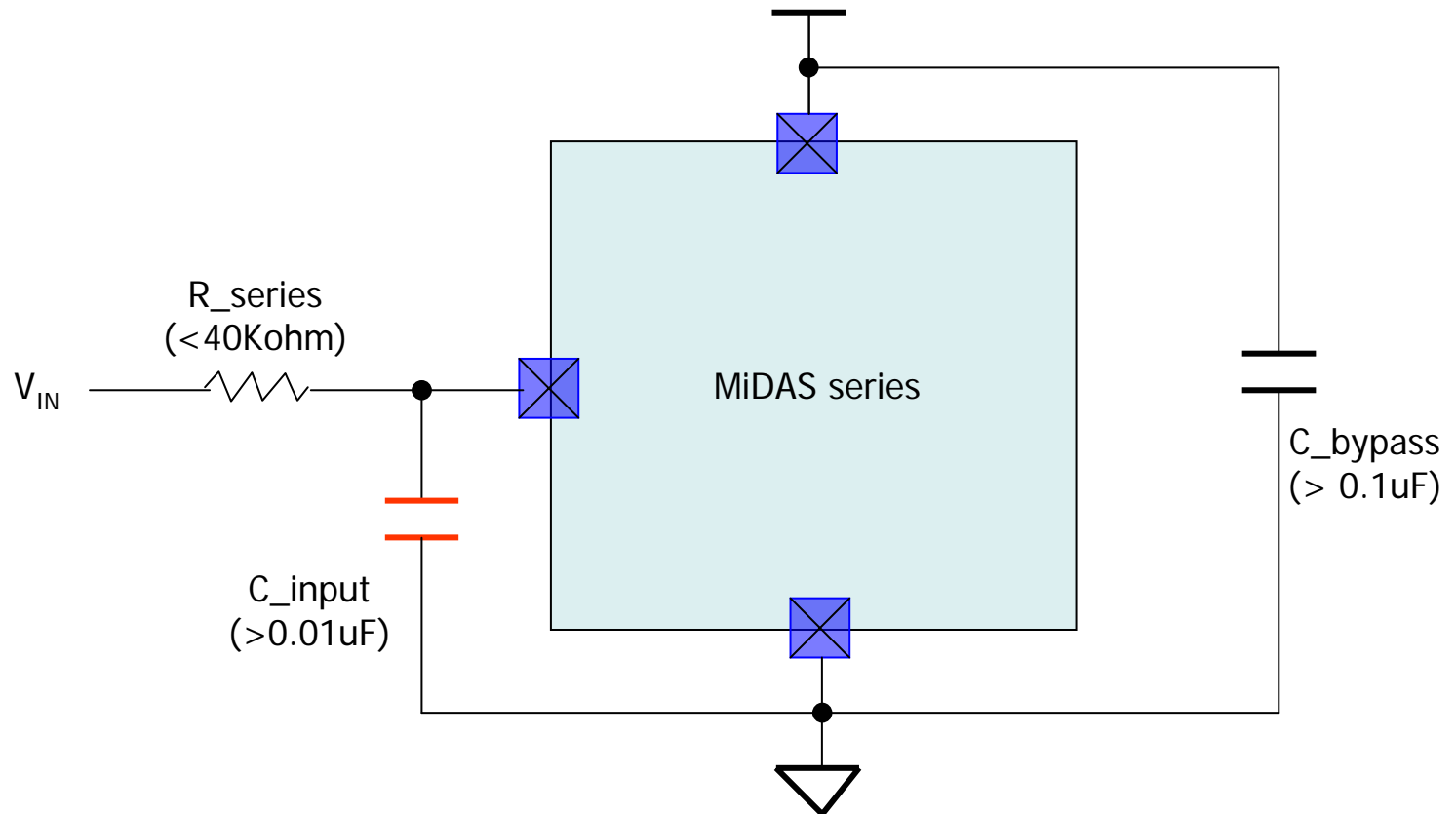
$$F_{ADC} = 50 \times 10^9 \times (1/R_E)$$

(If series resistor is selected by your application,

ADC sampling frequency is determined by the upper relationship.)

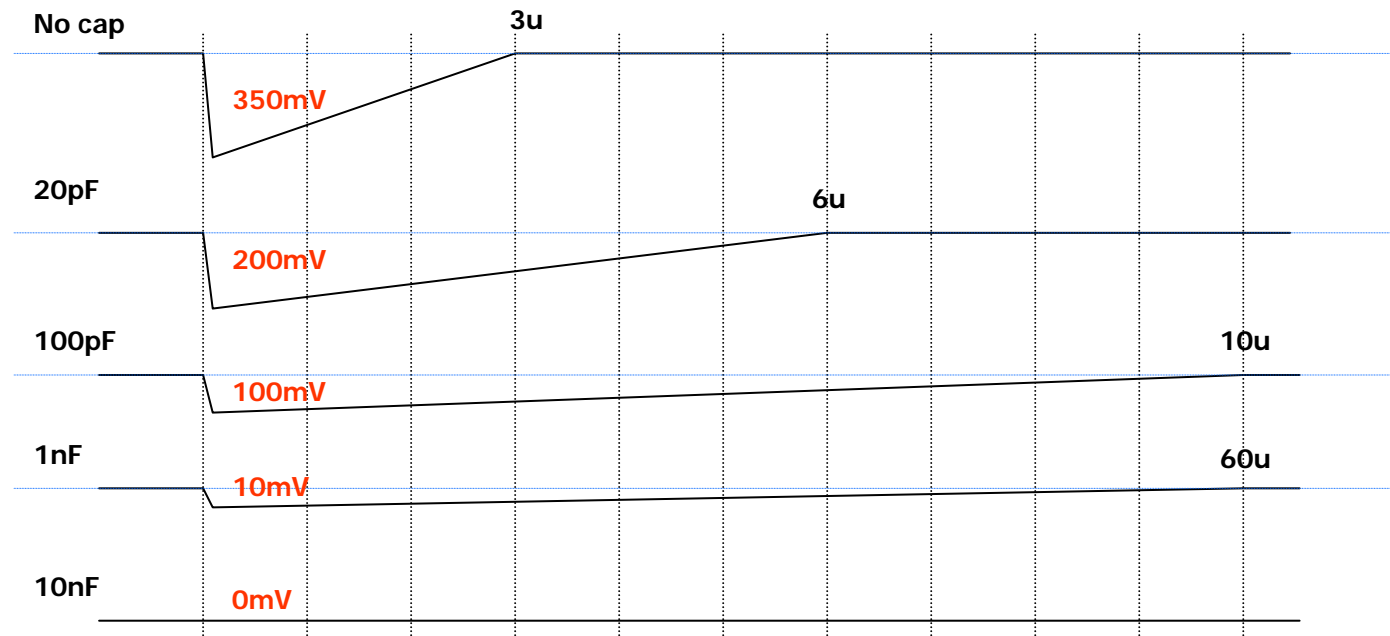
4. Input capacitor at input node

- ◆ Adding the input capacitor (system diagram)



4.1. Experiments and Analysis

◆ ADC input value by the input capacitance (30Kohm/4V input)



- * If C_{input} is 1nF, difference of output is about 2 code
- * If C_{input} is over 10nF, ADC input have no AC drop condition and stable output
- * If ADC input is DC value and 10nF capacitor, it has a good result

5. Remarks, and Recommendations

1. The reason of ADC output difference by the series resistance
 - 1) When ADC start signal is enabled, V_A node is dropped abruptly because of a internal resistors and capacitors.
 - 2) but ADC input current is limited by the series resistance, that is, the input recovery time is long.
 - 3) That moment, if the sampling is done, the output will not have a right value.
 - 4) Larger resistor, larger difference
 - 5) Faster sampling frequency, larger difference

2. Recommendations

If you use a big resistor, and then make a good results

- 1) Divide ADC sampling frequency
- 2) Set the input capacitor at ADC input node

In order to get more exact SFR value,

You'd better reset ADCR to 0x00 after using ADC function.

Appendix : Update History

- ◆ V1.1
 - ✓ Page 10
 - Recommendations Update