AN

MiDAS220 Application Guide for MiDAS1.1 Users

V1.0

Aug. 16, 2011

Product Overview

A. Brief Comparison Table for Device Family

Family	EPROM [Byte]	FLASH [Byte]	EEPROM [Byte]	RAM [Byte]	Volt [V]	Freq [MHz]	T/C [16 bits]	COM I/O	WDT	ADC (bit X Ch)	PWM (bit X ch)	I/O Pins	Package	Others	Available Time
MiDAS1.1	4K			128	2.4 ~ 5.5	10 (20)	2	1 UART	1	10 X 12 10 X 8 10 X 3	8 X 1	18 14 6	20-SOP 16-TSSOP 8-SOP	POR Ring OSC	**Now**
MiDAS230	-	2K	(128)	128	2.4 ~ 5.5	12 (24)	2	-	1	10 X 12 10 X 8 10 X 3	8 X 1	18 14 6	20-SOP 16-TSSOP 8-SOP	IAP ISP EJTAG LVD POR POSC	**Now**
MiDAS220		8K	(128)	128	2.2 ~ 5.5	12 (24)	2	1 UART 1 I2C	1	10 X 16 10 X 12 10 X 5	10 X 1	18 14 6	20-SOP 16-SOP 8-SOP	IAP ISP EJTAG LVD POR POSC ST	**`11, Q4**

◆ Product Family Tree

MiDAS1.1 → **MiDAS230**
↓ ↘ ↓
MiDAS2.2 → **MiDAS220**

1.1 Strong Points of MiDAS220 vs. MiDAS1.1

- Embedded FLASH with ISP (In System Programming)
  - ✓ The code memory of MiDAS220 is FLASH memory, while that of MiDAS1.1 is EPROM(OTP).
  - ✓ The embedded FLASH memory with ISP provides the maximum flexibility to production and logistics system.
    - Easy stock management for the small quantity batch production
    - The repair of code write failure at production line
    - The change of final product by changing embedded firmware before shipment
    - Upgrade of firmware at the customer service center
- Embedded EEPROM with IAP (In Application Programming)
  - ✓ Critical data for the application system can be easily stored with IAP in non-volatile EEPROM memory while application system is operating.
  - ✓ Self upgrade of application firmware by receiving command and data through serial communication channel.
  - ✓ Data retention : More than 10 years, Endurance : More than 100,000 cycles
- Internal precision oscillator with factory calibration
  - ✓ Provides stable clock against the variation of temperature and power supply voltage
  - ✓ Typical deviation is ±1 % and the maximum deviation is ±2 %.
  - ✓ The UART can safely operate with internal clock.
- Configurable LVD (Low Voltage Detector) with factory calibration
  - ✓ The internal LVD provides reset or interrupt to MCU against abnormal power condition.
  - ✓ The available range of LVD voltage is from 2.1V to 2.7V.
  - ✓ The resolution of calibration is 0.1V, which yields the maximum error as ±0.05V.
- Low power Operation Support
  - ✓ Wake-up from the power-down mode by external interrupts or i2c communication
  - ✓ Low power Stop Timer for self-wake-up from the power-down mode
  - ✓ Selective enable of peripheral clocks for low power operation

1.2 Comparison of MiDAS220 vs. MiDAS1.1

◆ Introduction

- ✓ MiDAS220 is an extended version of MiDAS230 which inherits most of the MiDAS1.1 features except a few differences.
- ✓ Most of the electrical characteristics are similar to each other.
- ✓ However, the migration feasibility should be tested with samples.
- ✓ Please refer to the manuals of MiDAS220 for the detailed description of common features.

◆ List of Differences (Changes)

Item	MiDAS220	MiDAS1.1
Code Memory	FLASH 8K Byte	EPROM 4K Byte
Program with ISP	More than 100,000 times	Only one time
Internal Clock	Precision OSC (±2 %), Freq = 461KHz ~ 11MHz	Ring OSC (±15 %), Freq = 456KHz ~ 3.65MHz
Power on reset / LVD	POR (1.6V) and Configurable LVD (2.1V ~ 2.7V)	POR (2.3V)
I/O ports initialization time	Initialized asynchronously by POR.	Initialized by synchronous internal reset.
I/O ports pull-up	I_{OHP} = -49uA @V_{DD}=5V,Pull-up is off when reset.	I_{OHP} = -140uA @V_{DD}=5V, Pull-up is on when reset.
I/O ports drive strength	I_{OL} = 17mA @V_{DD}=5V, I_{OH} = -18mA @V_{DD}=5V	I_{OL} = 20mA @V_{DD}=5V, I_{OH} = -15mA @V_{DD}=5V
WDT	Overflow count : 2^{19}, 2^{20}, 2^{21}, 2^{22}	Overflow count : 2^{16}, 2^{18}, 2^{20}, 2^{21}
ADC	Included clock divider, Max. divide ratio = 8 Num. of channel = 16	Share clock divider of PWM, Max. divide ratio = 128 Num. of channel = 12
High speed PWM	10-bit or 8-bit	8-bit only
Reset	External reset hold time is min. 20 us. Once triggered, internal reset holds 18 ms.	External reset hold time is min. 24 clocks. Once triggered, internal reset holds several clocks.

1.3 Comparison of MiDAS220 vs. MiDAS1.1

◆ List of Differences (New)

✓ Please refer to the manuals of MiDAS220 for the detailed description of new features.

Item	MiDAS220	MiDAS1.1
I2C Communication	1 channel, I2C start-bit can wake-up the power-down mode	Not Available
Embedded EEPROM with IAP	128 Byte (Part of Code Memory)	Not Available
Configurable P0[3:0] high current drive	I_{OL2} = 50mA @V_{DD}=5V, I_{OH2} = -26mA @V_{DD}=5V	Not Available
External Interrupt	Configuration for low/high polarity and edge/level selection	Not Available
Stop Timer	Low power timer with 32 KHz internal oscillator to wake-up from the power-down mode	Not Available
Peripheral clock enables	Selective enable of peripheral clocks for low power operation	Not Available
Timer0/1 count period selection	Select 12 clocks or 4 clocks	Not Available

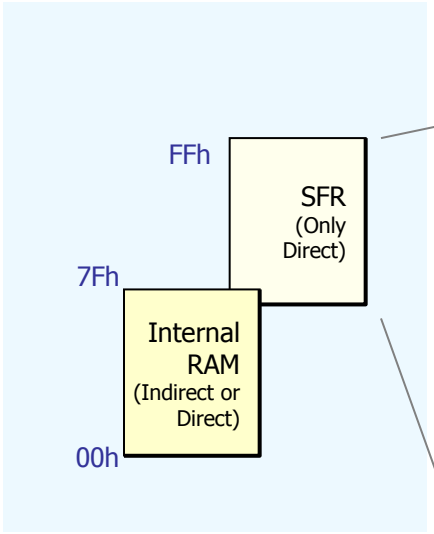
◆ Initialization routines for MiDAS230/MiDAS220

```
// Read the calibration data for Precision
// Oscillator from OTP area.
void init_posc(void)
{
  DPH     = 0;
  DPL     = 2;          // Low  byte of the address
  IAPCON  = 0x0D;       // Read byte in OTP
  RINGCON = IAPDAT;     // Read result

  DPL    += 2;          // Increment the address
  IAPCON  = 0x0D;       // Read byte in OTP
  OSCBIAS = IAPDAT;     // Read result

  DPL    += 2;          // Increment the address
  IAPCON  = 0x0D;       // Read byte in OTP
  OSCREF  = IAPDAT;     // Read result
}
```

```
// If reset is required at the same level as
// MiDAS1.1, use following routine
void init_lvd_reset(void)
{
  DPH     = 0;
  DPL     = 8;          // Data address
  IAPCON  = 0x0D;       // Read byte in OTP
  LVDCFG  = IAPDAT;     // Configuration for 2.4V
  LVDCFG -= 1;          // Configuration for 2.3V
  LVDCFG |= 0x80;       // Enable LVD Reset
}
```

Appendix.1 SFR (Special Function Register) Map

SFR	: Common basic 8051 SFR	SFR	: Unique SFR in MiDAS220 Family
SFR	: Common SFR in MiDAS220 and MiDAS1.1 Family		: Reserved for future use.



Bit addressable

F8h	EIP				IAPWEN	IAPCON	IAPDAT		FFh
F0h	B				P0DIR	P1DIR	P2DIR		F7h
E8h	EIE				P0HD		ADCR	ADCON	EFh
E0h	ACC	ADCSELH	ADCSEL	ALTSEL	P0SEL	P1SEL	P2SEL		E7h
D8h	WDCON	ADCHL		ADCHSEL	PWMCON	PWMDH	PWMD		DFh
D0h	PSW				P0TYPE	P1TYPE	P2TYPE		D7h
C8h	I2CST1	I2CSTH1		I2CCON1	I2CCFG1	I2CSLA1	I2CDAT1		CFh
C0h					PMR	STATUS	LVDCFG		C7h
B8h	IP				STCON	STCFG	OSCICN		BFh
B0h									B7h
A8h	IE								AFh
A0h	P2								A7h
98h	SCON	SBUF							9Fh
90h	P1	EXIF	PCLKEN		OSCTEST	RINGCON	OSCBIAS	OSCREF	97h
88h	TCON	TMOD	TL0	TL1	TH0	TH1	CKCON		8Fh
80h	P0	SP	DPL	DPH			ITSEL	PCON	87h

Appendix.2 I/O Ports

◆ MiDAS1.1

✓ P0SEL (E4h) : Port 0 Pull-up Control Register

P0SEL.7	P0SEL.6	P0SEL.5	P0SEL.4	P0SEL.3	P0SEL.2	P0SEL.1	P0SEL.0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

- 0 = Pull-up resistor ON (Default)
- 1 = Pull-up resistor OFF when ADC_EN (ADCON[7]) = 1

✓ P1SEL (E5h) : Port 1 Pull-up Control Register

-	-	-	-	-	-	P1SEL.1	P1SEL.0
						R/W(1)	R/W(1)

- 0 = Pull-up resistor ON
- 1 = Pull-up resistor OFF (Default)

✓ P2SEL (E6h) : Port 2 Pull-up Control Register

-	P2SEL.6	P2SEL.5	P2SEL.4	P2SEL.3	P2SEL.2	P2SEL.1	P2SEL.0
	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

- 0 = Pull-up resistor ON
- 1 = Pull-up resistor OFF when ADC_EN(ADCON[3]) = 1.

◆ MiDAS220

✓ P0SEL (E4h) : Port 0 Pull-up Control Register

P0SEL.7	P0SEL.6	P0SEL.5	P0SEL.4	P0SEL.3	P0SEL.2	P0SEL.1	P0SEL.0
R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(0)	R/W(0)

- 0 = Pull-up resistor ON / 1 = Pull-up resistor OFF

✓ P1SEL (E5h) : Port 1 Pull-up Control Register

-	-	-	-	-	P1SEL.2	P1SEL.1	P1SEL.0
					R/W(0)	R/W(1)	R/W(1)

- 0 = Pull-up resistor ON / 1 = Pull-up resistor OFF

✓ P2SEL (E6h) : Port 2 Pull-up Control Register

-	P2SEL.6	P2SEL.5	P2SEL.4	P2SEL.3	P2SEL.2	P2SEL.1	P2SEL.0
	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)

- 0 = Pull-up resistor ON / 1 = Pull-up resistor OFF (Default)

✓ P0HD (ECh) : Port 0 High Current Driving Register

-	-	-	-	P0HD.3	P0HD.2	P0HD.1	P0HD.0
				R/W(0)	R/W(0)	R/W(0)	R/W(0)

- 0 = Normal Current Driving (default) / 1 = High Current Driving

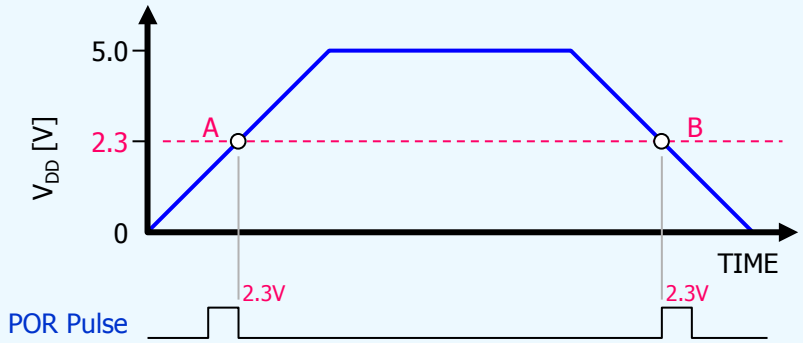
Appendix.3 POR / LVD

MiDAS1.1

✓ PCON (87h) : Power Control Register

SMOD1	-	-	POF	GF1	GF0	PD	IDL
R/W(0)			R/W(1)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

- POF : Power Off flag. When power-on, POF = 1 by H/W.
- PD : Power-down mode bit



MiDAS220

✓ LVDCFG (C6h) : LVD Configuration Register

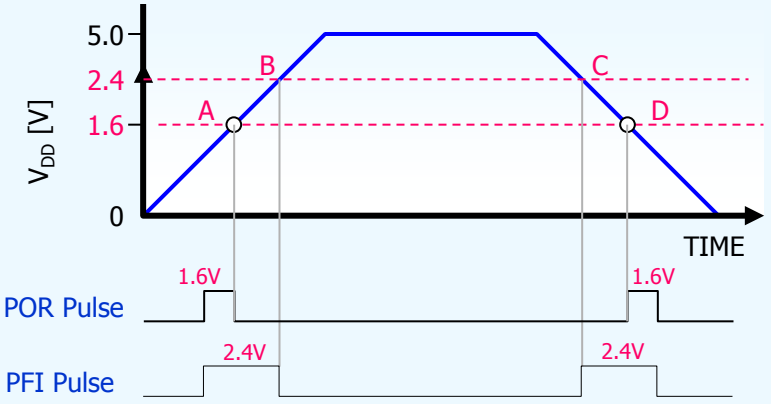
EPFR	EPFI	PFI	CFG4	CFG3	CFG2	CFG1	CFG0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R(1)	R/W(0)	R/W(1)

- EPFR : Power-fail reset enable.
- EPFI : Power-fail interrupt enable.
- PFI : Power-fail interrupt flag.
- CFG[4:0] : LVD Voltage Configuration

✓ PCON (87h) : Power Control Register

SMOD1	-	-	POF	GF1	GF0	PD	IDL
R/W(0)			R/W(1)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

- POF : Power off flag.
  When power-on, this flag bit will be set by H/W.
- PD : Power-down (Stop) mode enable.



Appendix.4 WDT (Watch Dog Timer)

MiDAS1.1

✓ WDCON (D8h) : Watchdog Timer Control Register

WD1	WD0	-	-	WDIF	WTRF	EWT	RWT
R/W(1)	R/W(1)	R/W(0)	R/W(1)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

- WD[1:0]: WDT Clock Divide(1/4/8/32)
- WDIF : Watchdog Timer Interrupt Flag
- WTRF : Watchdog Timer Reset Flag. Only cleared by S/W.
- EWT : Watchdog Timer Reset Enable
- RWT : Restart Watchdog Timer

WD1	WD0	Interrupt Time-out (@4MHz)		Reset Time-out
0	0	$1x2^{16}$ clocks	16.38 ms	$1x2^{16}$ + 256 clocks
0	1	$4x2^{16}$ clocks	65.54 ms	$4x2^{16}$ + 256 clocks
1	0	$16x2^{16}$ clocks	262.14 ms	$16x2^{16}$ + 256 clocks
1	1	$32x2^{16}$ clocks	524.29 ms	$32x2^{16}$ + 256 clocks

MiDAS230/MiDAS220

✓ WDCON (D8h) : Watchdog Timer & Power Status Register

WD1	WD0	WDM	-	WDIF	WTRF	EWT	RWT
R/W(1)	R/W(1)	R/W(0)	R(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

- WD[1:0]: WDT Clock Divide
- WDM : Watchdog clock divide mode for Test (Do not set this bit in the application.)
- WDIF : Watchdog Timer Interrupt Flag
- WTRF : Watchdog Timer Reset Flag
- EWT : Watchdog Timer Reset Enable
- RWT : Restart Watchdog Timer

WD1	WD0	Interrupt Time-out (@ 4MHz)		Reset Time-out
0	0	2^{19} clocks	131 ms	2^{19} + 512 clocks
0	1	2^{20} clocks	262 ms	2^{20} + 512 clocks
1	0	2^{21} clocks	524 ms	2^{21} + 512 clocks
1	1	2^{22} clocks	1048 ms	2^{22} + 512 clocks

Appendix.5 PWM (Pulse Width Modulator)

MiDAS1.1

✓ PWMCON (DCh) : PWM Control Register

P0SEL	PS2_P0	PS1_P0	PS0_P0	-	PWMF	CLR_P0	RUN_P0
R/W(0)	R/W(0)	R/W(0)	R/W(0)		R/W(0)	R/W(0)	R/W(0)

- P0SEL : PWM Waveform Output Enable to P0.6
- PS2_P0, PS1_P0, PS0_P0: Pre-scaled Clock Selection.
  [0,0,0] = $F_{OSC}/1$, [0,0,1] = $F_{OSC}/2$, [0,1,0] = $F_{OSC}/4$,
  [0,1,1] = $F_{OSC}/8$, [1,0,0] = $F_{OSC}/16$, [1,0,1] = $F_{OSC}/32$,
  [1,1,0] = $F_{OSC}/64$, [1,1,1] = $F_{OSC}/128$
  * PWM Clock (F_{PWM}) to ADC should not be set to $F_{OSC}/1$.
- PWMF : PWM Interrupt Flag. Cleared by S/W
- CLR_P0 : Counter Reset Enable. Cleared by H/W.
- RUN_P0 : Counter Start Enable.

MiDAS220

✓ PWMCON (DCh) : PWM Control Register

PWM06	PS2_P0	PS1_P0	PS0_P0	PWMM	PWMF	CLR_P0	RUN_P0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

- PWM06 : PWM Waveform Output Enable to P0.6
- PS2_P0, PS1_P0, PS0_P0: Pre-scaled Clock Selection.
  [0,0,0] = $F_{SYS}/1$, [0,0,1] = $F_{SYS}/2$, [0,1,0] = $F_{SYS}/4$,
  [0,1,1] = $F_{SYS}/8$, [1,0,0] = $F_{SYS}/16$, [1,0,1] = $F_{SYS}/32$,
  [1,1,0] = $F_{SYS}/64$, [1,1,1] = $F_{SYS}/128$
  If PWMM is set, maximum pre-scale ratio is $F_{SYS}/32$.
- PWMM : PWM Mode Select
  [0] : 8-bit PWM, [1] : 10-bit PWM
- PWMF : PWM Interrupt Flag. Cleared by S/W
- CLR_P0 : Counter Reset Enable. Cleared by H/W.
- RUN_P0 : Counter Start Enable.

✓ PWMDH (DDh) : PWM Duty Data High Register

-	-	-	-	-	-	PWMDH.1	PWMDH.0
						R/W(0)	R/W(0)

Appendix.6 ADC (Analog-to-Digital Converter)

MiDAS1.1

■ **ADCON** (EFh) : ADC Control & ADC Result Low Register : Value[1:0]

AD_EN	AD_REQ	AD_END	ADCF	AVREF	ADIV	SAR1	SAR0
R/W(0)	R/W(0)	R(1)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

- AD_EN : ADC ready enable.
- AD_REQ : ADC start.
  Cleared by H/W when AD_END goes to 1 from 0.
- AD_END : Current ADC status.
  0 = ADC is running now.
- ADCF : ADC interrupt flag. Must be cleared by S/W.
- AVREF : 1 = ADC reference voltage enable from P0.4.
- ADIV : ADC input clock select
  0 = System clock (F_{OSC}) / 2. (Default)
  1 = PWM input clock (F_{PWM})
- SAR1, SAR0 : Low bits of ADC result value.

MiDAS220

■ **ADCON** (EFh) : ADC Control & ADC Result Low Register : Value[1:0]

AD_EN	AD_REQ	AD_END	ADCF	ADIV1	ADIV0	SAR1	SAR0
R/W(0)	R/W(0)	R(1)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

- AD_EN : ADC ready enable.
- AD_REQ : ADC start.
  Cleared by H/W when AD_END goes to 1 from 0.
- AD_END : Current ADC status.
  0 = ADC is running now.
- ADCF : ADC interrupt flag. Must be cleared by S/W.
- ADIV1, ADIV0 : ADC input clock select.
  [0,0] = System clock (F_{SYS}) / 2 (Default)
  [0,1] = System clock (F_{SYS}) / 4
  [1,0] = System clock (F_{SYS}) / 8
  [1,1] = System clock (F_{SYS})
- SAR1, SAR0 : Low bits of ADC result value.

■ **ADCHL** (D9h) : ADC High Channel Selection Low Register

ADCH7B	-	-	-	ADCH3B	ADCH2B	-	ADCH0B
R/W(1)				R/W(1)	R/W(1)		R/W(1)

- ADCHXB = 0 : ADCHX input enable (Digital input disable)

■ **ADCHSEL** (DBh) : ADC High Channel Selection Register

CH_SEL	-	-	-	-	CHH2	CHH1	CHH0
R/W(0)					R/W(0)	R/W(0)	R/W(0)

- CH_SEL : ADC MUX Selector with CHH[2:0] & CH[3:0].
  0 = CH[3:0] ADC[11:0] Enable / ADCH[7:0] Disable (Default)
  1 = CHH[2:0] ADC[11:0] Disable/ ADCH[7:0] Enable
- CHH[3:0] : ADC MUX Selection for High Channel

Appendix.7 Interrupt

- MiDAS1.1

HIGH

Interrupt Sources	Address	Priority Level
$\overline{\text{INT0}}$	0003h	2 Levels
TF0	000Bh	2 Levels
$\overline{\text{INT1}}$	0013h	2 Levels
TF1	001Bh	2 Levels
RI+TI	0023h	2 Levels
ADC	003Bh	2 Levels
INT2	0043h	2 Levels
INT3	004Bh	2 Levels
WDT	0063h	2 Levels
PWM	006Bh	2 Levels

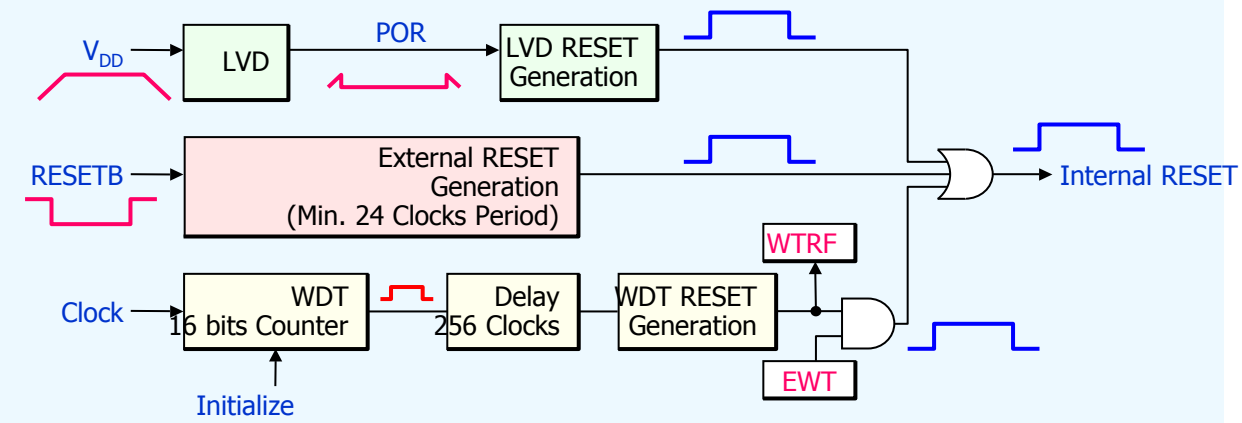
- MiDAS220

HIGH

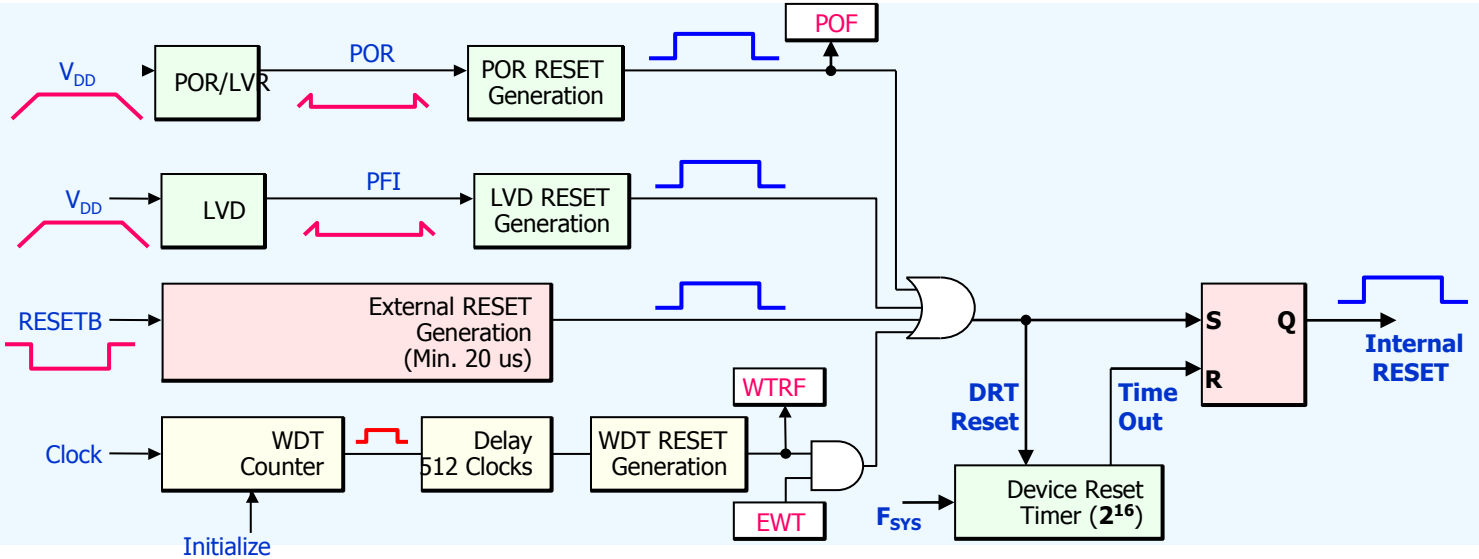
Interrupt Sources	Address	Priority Level	
LVD	0033h	Highest	NMI
INT0	0003h	2 Levels	
TF0	000Bh	2 Levels	
INT1	0013h	2 Levels	
TF1	001Bh	2 Levels	
RI+TI	0023h	2 Levels	
ADC	003Bh	2 Levels	
INT2	0043h	2 Levels	
INT3	004Bh	2 Levels	
I2C1	005Bh	2 Levels	
WDT	0063h	2 Levels	
PWM	006Bh	2 Levels	

Appendix.8 Reset Circuit

- MiDAS1.1



- MiDAS230 /MiDAS220



Appendix.9 Clock Circuit

MiDAS1.1

EXIF (91h) : External Interrupt Flag Register

-	-	IE3	IE2	XT/RG	RGMD	RGSL	BGS
		R/W(0)	R/W(0)	R/W(0)	R(1)	R/W(0)	R/W(1)

- IE3 : External interrupt 3 flag. Cleared by S/W.
- IE2 : External interrupt 2 flag. Cleared by S/W.
- XT/RG : System clock selection
  0 = Internal Ring oscillator is selected as system clock.
  1 = External clock is selected as system clock.
- RGMD : Ring mode. Now system clock is Ring or XTAL.
  Generally RGMD is the invert of XT/RG.
- RGSL : Ring select bit when power-down wake-up.
  1 = When wake-up from power-down mode in XTAL clock, use Ring oscillator as system clock during 65,536 XTAL clocks.
- BGS : Band-gap select. (Default = 1)
  0 = Band-gap block (LVD) will do not run in power-down mode, but function during normal mode.
  It will support the significant power savings in power-down mode.
  1 = Band-gap block (LVD) will run in power-down mode.

Control Flag				System Clock	Status Bit	
XT/RG	XTOFF	RINGON	RGSL		RGMD	XTUP
1	0	X	X	Crystal OSC.	0	1
0	X	1	X	Ring OSC.	1	0/1
1	0	X	0	Crystal OSC. (during Power-down Wake-up)	0	0
0	X	1	1	Ring OSC. (during Power-down Wake-up)	1	0

MiDAS220

EXIF (91h) : External Interrupt Flag Register

-	-	IE3	IE2	XT/RG	RGMD	RGSL	BGS
		R/W(0)	R/W(0)	R/W(0)	R(1)	R(1)	R/W(1)

- IE3 : External interrupt 3 flag. IT3 = ITSEL.7
  If IT3 = 0, cleared by S/W (software).
  If IT3 = 1, cleared automatically when go to routine.
- IE2 : External interrupt 2 flag . IT2 = ITSEL.6
  If IT2 = 0, cleared by S/W (software).
  If IT2 = 1, cleared automatically when go to routine.
- XT/RG : System clock selection.
  0 = Internal Ring oscillator is selected as system clock.
  1 = External clock is selected as system clock.
- RGMD : Ring mode. Now system clock is RCLK.
  Generally RGMD is the invert of XT/RG.
- RGSL : Ring select bit when power-down wake-up.
  When wake-up from power-down mode in XTAL clock, use RCLK as system clock during 65,536 RCLK cycles.
  This bit is always 1.
- BGS : Band-gap select. (Default = 1)
  0 = Band-gap block (POR) will do not run in power-down mode, but function during normal mode.
  It will support the significant power savings in power-down mode.
  1 = Band-gap block (POR) will run in power-down mode.

Control Flag			System Clock	Status Bit	
XT/RG	XTOFF	RINGON		RGMD	XTUP
1	0	X	Crystal OSC.	0	1
1	0	X	Precision OSC. (wake-up from power-down)	1	0
0	X	1	Precision OSC.	1	0/1

Appendix.9 Clock Circuit (cont'd)

MiDAS1.1

■ **OSCICN** (BEh) : Internal Ring Oscillator Control Register

-	-	-	-	-	RINGON	DIV1	DIV0
					R/W(1)	R/W(0)	R/W(0)

- RINGON : 1 = Internal ring oscillator is running.
  0 = Internal ring oscillator is killed.
  Don't clear RINGON bit when XTRG = 0.
- DIV1, DIV0 : Ring oscillator divider.
  [0,0] = 3.65MHz/1
  [0,1] = 3.65MHz/2
  [1,0] = 3.65MHz/4
  [1,1] = 3.65Mhz/8

MiDAS230/MiDAS220

■ **OSCICN** (BEh) : Internal Oscillator Control Register

-	-	-	-	DIV2	RINGON	DIV1	DIV0
				R/W(0)	R/W(1)	R/W(0)	R/W(0)

- RINGON : 1 = Internal Precision Oscillator(11 MHz) is running.
  0 = Internal Precision Oscillator is killed.
  Don't clear RINGON bit when XTRG = 0.
- DIV2, DIV1, DIV0 : Internal oscillator divider
  [0,0,0] = 3.68 MHz = F_{POSC} / 3 ; Default
  [0,0,1] = 1.84 MHz = F_{POSC} / 6
  [0,1,0] = 922 KHz = F_{POSC} / 12
  [0,1,1] = 461 KHz = F_{POSC} / 24
  [1,0,0] = reserved
  [1,0,1] = 11.06 MHz = F_{POSC}
  [1,1,0] = 5.53 MHz = F_{POSC} / 2
  [1,1,1] = 2.76 MHz = F_{POSC} / 4

✓ RINGCON(95h) : Internal Oscillator Frequency Tuning

S7	S6	S5	S4	S3	S2	S1	S0
R/W(1)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

✓ OSCBIAS(96h) : Internal Oscillator Bias Current Tuning

BIAS.7	BIAS.6	BIAS.5	BIAS.4	BIAS.3	BIAS.2	BIAS.1	BIAS.0
R/W(0)	R/W(1)	R/W(0)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)

✓ OSCREF(97h) : Internal Oscillator Reference Tuning

-	-	-	OREF.4	OREF.3	OREF.2	OREF.1	OREF.0
			R/W(1)	R/W(0)	R/W(1)	R/W(1)	R/W(1)

Final Comment

- The contents in this note is provided for quick reference.
- Please refer to the manuals of MiDAS220 and MiDAS1.1 for detailed descriptions.

Thank you !!!