



MiDAS Family

Application Note #059

(AN059-V1.0)



MiDAS220 Application Guide for MiDAS2.2 Users

V1.0

Aug. 16, 2011

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Product Overview

A. Brief Comparison Table for Device Family

| Family | EPROM [Byte] | FLASH [Byte] | EEPROM [Byte] | RAM [Byte] | Volt [V] | Freq [MHz] | T/C [16 bits] | COM I/O | WDT | ADC (bit X Ch) | PWM (bit X ch) | I/O Pins | Package | Others | Available Time |
|----------|--------------|--------------|---------------|------------|-----------|------------|---------------|-----------------|-----|------------------------------|----------------|---------------|-----------------------------|---|----------------|
| MiDAS1.1 | 4K | | | 128 | 2.4 ~ 5.5 | 10 (20) | 2 | 1 UART | 1 | 10 X 12 10 X 8 10 X 3 | 8 X 1 | 18 14 6 | 20-SOP 16-TSSOP 8-SOP | POR Ring OSC | Now |
| MiDAS230 | - | 2K | (128) | 128 | 2.4 ~ 5.5 | 12 (24) | 2 | - | 1 | 10 X 12 10 X 8 10 X 3 | 8 X 1 | 18 14 6 | 20-SOP 16-TSSOP 8-SOP | IAP ISP EJTAG LVD POR POSC | Now |
| MiDAS2.2 | - | 4K | (128) | 128 | 2.2 ~ 5.5 | 6 (12) | 2 | 1 UART 2 I2C | 1 | 10 X 16 10 X 12 10 X 5 | 8 X 1 | 18 14 6 | 20-SOP 16-SOP 8-SOP | IAP ISP EJTAG LVD POR Ring OSC | Now |
| MiDAS220 | | 8K | (128) | 128 | 2.2 ~ 5.5 | 12 (24) | 2 | 1 UART 1 I2C | 1 | 10 X 16 10 X 12 10 X 5 | 10 X 1 | 18 14 6 | 20-SOP 16-SOP 8-SOP | IAP ISP EJTAG LVD POR POSC ST | '11, Q4 |

◆ Product Family Tree



1.1 Strong Points of MiDAS220 vs. MiDAS2.2

◆ High Operation Frequency

- ✓ M220 is twice faster than MiDAS2.2.
- ✓ Even at the lowest operation voltage (2.2V), MiDAS220 can run at the maximum frequency of internal clock (11 MHz).

◆ Embedded FLASH with ISP (In System Programming)

- ✓ New write enable register greatly enhances the protection of FLASH contents at unstable power supply conditions.

◆ Embedded EEPROM with IAP (In Application Programming)

- ✓ Simplified IAP interface.
- ✓ IAP operation is guaranteed at wider range of power supply voltage (2.4V ~ 5.5V)

◆ Internal precision oscillator with factory calibration

- ✓ Provides stable clock against the variation of temperature and power supply voltage
- ✓ Typical deviation is $\pm 1\%$ and the maximum deviation is $\pm 2\%$.
- ✓ The UART can safely operate with internal clock.

◆ Configurable LVD (Low Voltage Detector) with factory calibration

- ✓ The internal LVD provides reset or interrupt to MCU against abnormal power condition.
- ✓ The available range of LVD voltage is from 2.1V to 2.7V.
- ✓ The resolution of calibration is 0.1V, which yields the maximum error as $\pm 0.05V$.

◆ Low power Operation Support

- ✓ Wake-up from the power-down mode by external interrupts or i2c communication
- ✓ Low power Stop Timer for self-wake-up from the power-down mode
- ✓ Selective enable of peripheral clocks for low power operation

1.2 Comparison of MiDAS220 vs. MiDAS2.2

◆ Introduction

- ✓ MiDAS220 inherits most of the MiDAS2.2 features except a few differences.
- ✓ Most of the electrical characteristics are similar to each other.
- ✓ However, the migration feasibility should be tested with samples.
- ✓ Please refer to the manuals of MiDAS220 for the detailed description of common features.

◆ List of Differences (Changes & New Features)

| Item | MiDAS220 | MiDAS2.2 |
|----------------------------|--|---|
| Code Memory | FLASH 8K Byte | FLASH 4K Byte |
| Internal Clock | Precision OSC ($\pm 2\%$), Freq = 461KHz ~ 11MHz | Ring OSC ($\pm 15\%$), Freq = 456KHz ~ 3.65MHz |
| Power on reset / LVD | POR (1.6V) and Configurable LVD (2.1V ~ 2.7V) | POR (1.6V) and LVD (2.2V) |
| I/O ports pull-up | Pull-up is off when reset. | Pull-up is on when reset. |
| I/O ports drive strength | $I_{OL} = 17\text{mA} @V_{DD}=5\text{V}$, $I_{OH} = -18\text{mA} @V_{DD}=5\text{V}$ | $I_{OL} = 20\text{mA} @V_{DD}=5\text{V}$, $I_{OH} = -15\text{mA} @V_{DD}=5\text{V}$ |
| P0[3:0] high current drive | $I_{OL2} = 50\text{mA} @V_{DD}=5\text{V}$, $I_{OH2} = -26\text{mA} @V_{DD}=5\text{V}$ | Not Available |
| WDT | Not Available | Operation with 32KHz internal oscillator |
| Stop Timer | Low power timer with 32 KHz internal oscillator to wake-up from the power-down mode | Not Available |
| ADC | Included clock divider, Max. divide ratio = 8 | Share clock divider of PWM, Max. divide ratio = 128 |
| High speed PWM | 10-bit or 8-bit | 8-bit or 6-bit |
| I2C Communication | 1 channel (slave) with TX double buffer. I2C start-bit can wake-up the power-down mode | 2 channel (slave, master) |
| Reset | External reset hold time is min. 20 μs . Once triggered, internal reset holds 18 ms. | External reset hold time is min. 24 clocks. Once triggered, internal reset holds several clocks. |

1.3 Comparison of MiDAS220 vs. MiDAS2.2

◆ List of Differences (continued)

✓ Please refer to the manuals of MiDAS220 for the detailed description of new features.

| Item | MiDAS220 | MiDAS2.2 |
|---------------------------------|---|---------------|
| Peripheral clock enables | Selective enable of peripheral clocks for low power operation | Not Available |
| Timer0/1 count period selection | Select 12 clocks or 4 clocks | Not Available |

1.4 Firmware Guide for MiDAS220

◆ Initialization routines for MiDAS230/MiDAS220

```
// Read the calibration data for Precision
// Oscillator from OTP area.
void init_posc(void)
{
    DPH      = 0;
    DPL      = 2;          // Low byte of the address
    IAPCON   = 0x0D;      // Read byte in OTP
    RINGCON  = IAPDAT;    // Read result

    DPL     += 2;          // Increment the address
    IAPCON   = 0x0D;      // Read byte in OTP
    OSCBIAS  = IAPDAT;    // Read result

    DPL     += 2;          // Increment the address
    IAPCON   = 0x0D;      // Read byte in OTP
    OSCREF   = IAPDAT;    // Read result
}
```

```
// If reset is required at the same level as
// MiDAS1.1, use following routine
void init_lvd_reset(void)
{
    DPH      = 0;
    DPL      = 8;          // Data address
    IAPCON   = 0x0D;      // Read byte in OTP
    LVDCFG   = IAPDAT;    // Configuration for 2.4V
    LVDCFG  -= 1;          // Configuration for 2.3V
    LVDCFG  |= 0x80;      // Enable LVD Reset
}
```

Appendix.1 SFR (Special Function Register) Map

- SFR : Common basic 8051 SFR
- SFR : Unique SFR in MiDAS220 Family
- SFR : Common SFR in MiDAS220 and MiDAS2.2 Family
- SFR : Unique SFR in MiDAS2.2 Family

Bit addressable

| | | | | | | | | | |
|-----|--------|---------|--------|---------|---------|---------|---------|-------------|-----|
| F8h | EIP | EECNTLD | EECNTL | EECNTM | IAPWEN | IAPCON | IAPDAT | EEAEN | FFh |
| F0h | B | | | | P0DIR | P1DIR | P2DIR | | F7h |
| E8h | EIE | | | | P0HD | | ADCR | ADCON | EFh |
| E0h | ACC | ADCSELH | ADCSEL | ALTSEL | P0SEL | P1SEL | P2SEL | | E7h |
| D8h | WDCON | ADCHL | | ADCHSEL | PWMCON | PWMDH | PWMD | | DFh |
| D0h | PSW | WDMOD | | | P0TYPE | P1TYPE | P2TYPE | | D7h |
| C8h | I2CST1 | I2CSTH1 | | I2CCON1 | I2CCFG1 | I2CSLA1 | I2CDAT1 | | CFh |
| C0h | | | | | PMR | STATUS | LVDCFG | | C7h |
| B8h | IP | | | | STCON | STCFG | OSCICN | OSC2ICN | BFh |
| B0h | I2CST0 | | | I2CCON0 | I2CCFG0 | I2CSLA0 | I2CDAT0 | I2CI2CO_SCL | B7h |
| A8h | IE | | | | | | | | AFh |
| A0h | P2 | | | | | | | | A7h |
| 98h | SCON | SBUF | | | | | | | 9Fh |
| 90h | P1 | EXIF | PCLKEN | | OSCTEST | RINGCON | OSCBIAS | OSCREF | 97h |
| 88h | TCON | TMOD | TL0 | TL1 | TH0 | TH1 | CKCON | | 8Fh |
| 80h | P0 | SP | DPL | DPH | | | ITSEL | PCON | 87h |

Appendix.2 I/O Ports

◆ MiDAS2.2

✓ POSEL (E4h) : Port 0 Pull-up Control Register

| | | | | | | | |
|---------|---------|---------|---------|---------|---------|---------|---------|
| POSEL.7 | POSEL.6 | POSEL.5 | POSEL.4 | POSEL.3 | POSEL.2 | POSEL.1 | POSEL.0 |
| R/W(0) | R/W(0) | R/W(0) | R/W(0) | R/W(0) | R/W(0) | R/W(0) | R/W(0) |

- 0 = Pull-up resistor ON (Default)
- 1 = Pull-up resistor OFF when ADC_EN (ADCON[7]) = 1

✓ P1SEL (E5h) : Port 1 Pull-up Control Register

| | | | | | | | |
|---|---|---|---|---|---|---------|---------|
| - | - | - | - | - | - | P1SEL.1 | P1SEL.0 |
| | | | | | | R/W(1) | R/W(1) |

- 0 = Pull-up resistor ON
- 1 = Pull-up resistor OFF (Default)

✓ P2SEL (E6h) : Port 2 Pull-up Control Register

| | | | | | | | |
|--------|---------|---------|---------|---------|---------|---------|---------|
| - | P2SEL.6 | P2SEL.5 | P2SEL.4 | P2SEL.3 | P2SEL.2 | P2SEL.1 | P2SEL.0 |
| R/W(0) | R/W(0) | R/W(0) | R/W(0) | R/W(0) | R/W(0) | R/W(0) | R/W(0) |

- 0 = Pull-up resistor ON
- 1 = Pull-up resistor OFF when ADC_EN(ADCON[3]) = 1.

◆ MiDAS220

✓ POSEL (E4h) : Port 0 Pull-up Control Register

| | | | | | | | |
|---------|---------|---------|---------|---------|---------|---------|---------|
| POSEL.7 | POSEL.6 | POSEL.5 | POSEL.4 | POSEL.3 | POSEL.2 | POSEL.1 | POSEL.0 |
| R/W(1) | R/W(1) | R/W(1) | R/W(1) | R/W(1) | R/W(1) | R/W(0) | R/W(0) |

- 0 = Pull-up resistor ON / 1 = Pull-up resistor OFF

✓ P1SEL (E5h) : Port 1 Pull-up Control Register

| | | | | | | | |
|---|---|---|---|---|---------|---------|---------|
| - | - | - | - | - | P1SEL.2 | P1SEL.1 | P1SEL.0 |
| | | | | | R/W(0) | R/W(1) | R/W(1) |

- 0 = Pull-up resistor ON / 1 = Pull-up resistor OFF

✓ P2SEL (E6h) : Port 2 Pull-up Control Register

| | | | | | | | |
|--------|---------|---------|---------|---------|---------|---------|---------|
| - | P2SEL.6 | P2SEL.5 | P2SEL.4 | P2SEL.3 | P2SEL.2 | P2SEL.1 | P2SEL.0 |
| R/W(1) | R/W(1) | R/W(1) | R/W(1) | R/W(1) | R/W(1) | R/W(1) | R/W(1) |

- 0 = Pull-up resistor ON / 1 = Pull-up resistor OFF (Default)

✓ P0HD (ECh) : Port 0 High Current Driving Register

| | | | | | | | |
|---|---|---|---|--------|--------|--------|--------|
| - | - | - | - | P0HD.3 | P0HD.2 | P0HD.1 | P0HD.0 |
| | | | | R/W(0) | R/W(0) | R/W(0) | R/W(0) |

- 0 = Normal Current Driving (default) / 1 = High Current Driving

Appendix.3 POR / LVD

◆ MiDAS2.2

✓ WDCON (D8h) : Watchdog Timer Control Register

| | | | | | | | |
|--------|--------|--------|--------|--------|------|-----|--------|
| WD1 | WD0 | EPFI | PFI | WDIF | WTRF | EWT | RWT |
| R/W(1) | R/W(1) | R/W(0) | R/W(1) | R/W(0) | | | R/W(0) |

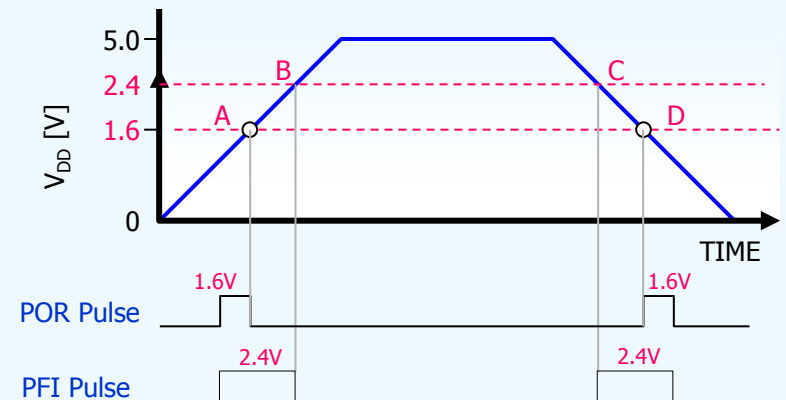
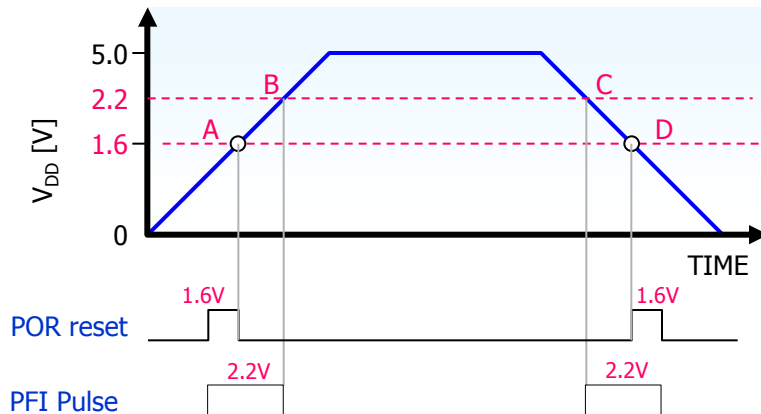
- EPFI : Power-fail interrupt enable.
- PFI : Power-fail interrupt flag.

◆ MiDAS230/MiDAS220

✓ LVDCFG (C6h) : LVD Configuration Register

| | | | | | | | |
|--------|--------|--------|--------|--------|------|--------|--------|
| EPFR | EPFI | PFI | CFG4 | CFG3 | CFG2 | CFG1 | CFG0 |
| R/W(0) | R/W(0) | R/W(0) | R/W(0) | R/W(0) | R(1) | R/W(0) | R/W(1) |

- EPFR : Power-fail reset enable.
- EPFI : Power-fail interrupt enable.
- PFI : Power-fail interrupt flag.
- CFG[4:0] : LVD Voltage Configuration



Appendix.4 WDT (Watch Dog Timer)

◆ MiDAS2.2

✓ WDCON (D8h) : Watchdog Timer & Power Status Register

| | | | | | | | |
|--------|--------|--------|--------|--------|--------|--------|--------|
| WD1 | WD0 | EPFI | PFI | WDIF | WTRF | EWT | RWT |
| R/W(1) | R/W(0) | R/W(1) | R/W(0) | R/W(0) | R/W(0) | R/W(0) | R/W(0) |

- WD[1:0]: WDT Clock Divide
- EPFI : Enable Power-fail Interrupt
- PFI : Power-Fail interrupt Flag
- WDIF : Watchdog Timer Interrupt Flag
- WTRF : Watchdog Timer Reset Flag
- EWT : Watchdog Timer Reset Enable
- RWT : Restart Watchdog Timer

✓ WDMOD (D1h) : Watchdog Mode register

| | | | | | | | |
|---|---|---|---|---|---|---|--------|
| - | - | - | - | - | - | - | WDM |
| | | | | | | | R/W(0) |

- WDM : Watchdog clock divide mode

| WDM | WD1 | WD0 | Interrupt Time-out | | Reset Time-out |
|---------------|-----|-----|------------------------|---------|------------------------------|
| 1 (@4MHz) | 0 | 0 | 2 ¹⁹ clocks | 131 ms | 2 ¹⁷ + 256 clocks |
| | 0 | 1 | 2 ²⁰ clocks | 262 ms | 2 ²⁰ + 256 clocks |
| | 1 | 0 | 2 ²¹ clocks | 524 ms | 2 ²³ + 256 clocks |
| | 1 | 1 | 2 ²² clocks | 1048 ms | 2 ²⁶ + 256 clocks |
| 0 (@32KHz) | 0 | 0 | 2 ⁹ clocks | 16 ms | 2 ⁹ + 256 clocks |
| | 0 | 1 | 2 ¹⁰ clocks | 32 ms | 2 ¹⁰ + 256 clocks |
| | 1 | 0 | 2 ¹¹ clocks | 64 ms | 2 ¹¹ + 256 clocks |
| | 1 | 1 | 2 ¹² clocks | 128 ms | 2 ¹² + 256 clocks |

◆ MiDAS230/MiDAS220

✓ WDCON (D8h) : Watchdog Timer & Power Status Register

| | | | | | | | |
|--------|--------|--------|------|--------|--------|--------|--------|
| WD1 | WD0 | WDM | - | WDIF | WTRF | EWT | RWT |
| R/W(1) | R/W(1) | R/W(0) | R(0) | R/W(0) | R/W(0) | R/W(0) | R/W(0) |

- WD[1:0]: WDT Clock Divide
- WDM : Watchdog clock divide mode for Test
(Do not set this bit in the application.)
- WDIF : Watchdog Timer Interrupt Flag
- WTRF : Watchdog Timer Reset Flag
- EWT : Watchdog Timer Reset Enable
- RWT : Restart Watchdog Timer

| WD1 | WD0 | Interrupt Time-out (@ 4MHz) | | Reset Time-out |
|-----|-----|-----------------------------|---------|------------------------------|
| 0 | 0 | 2 ¹⁹ clocks | 131 ms | 2 ¹⁹ + 512 clocks |
| 0 | 1 | 2 ²⁰ clocks | 262 ms | 2 ²⁰ + 512 clocks |
| 1 | 0 | 2 ²¹ clocks | 524 ms | 2 ²¹ + 512 clocks |
| 1 | 1 | 2 ²² clocks | 1048 ms | 2 ²² + 512 clocks |

Appendix.5 PWM (Pulse Width Modulator)

◆ MiDAS2.2

✓ PWMCON (DCh) : PWM Control Register

| | | | | | | | |
|-------|--------|--------|--------|---------|-------|--------|--------|
| POSEL | PS2_P0 | PS1_P0 | PS0_P0 | MODE_P0 | RL_P0 | CLR_P0 | RUN_P0 |
|-------|--------|--------|--------|---------|-------|--------|--------|

R/W(0) R/W(0) R/W(0) R/W(0) R/W(0) R/W(0) R/W(0) R/W(0)

- POSEL : PWM Waveform Output to Port.
- PS2_P0, PS1_P0, and PS0_P : Clock prescale ratio Selection.
 $F_{SYS}/1, /2, /4, /8, /16, /32, /64, /128$.
- MODE_P0 : 8-bit / (2+6)-bit Counter Mode Selector.
 MODE_P0=0, (2+6)-bit Mode
 MODE_P0=1, 8-bit Mode
- RL_P0 : PWM data update mode selector.
 RL_P0=0, update at 6-bit Counter Overflow.
 RL_P0=1, update at 8-bit Counter Overflow.
- CLR_P0 : Counter Reset Enable. Clear by H/W.
- RUN_P0 : Counter Start Enable.

✓ PWMIF (DDh) : PWM Interrupt Register

| | | | | | | | |
|---|---|---|---|---|---|---|-------|
| - | - | - | - | - | - | - | PWMIF |
|---|---|---|---|---|---|---|-------|

R/W(0)

◆ MiDAS220

✓ PWMCON (DCh) : PWM Control Register

| | | | | | | | |
|-------|--------|--------|--------|------|------|--------|--------|
| PWM06 | PS2_P0 | PS1_P0 | PS0_P0 | PWMM | PWMF | CLR_P0 | RUN_P0 |
|-------|--------|--------|--------|------|------|--------|--------|

R/W(0) R/W(0) R/W(0) R/W(0) R/W(0) R/W(0) R/W(0) R/W(0)

- PWM06 : PWM Waveform Output Enable to P0.6
- PS2_P0, PS1_P0, PS0_P0: Pre-scaled Clock Selection.
 $[0,0,0] = F_{SYS}/1, [0,0,1] = F_{SYS}/2, [0,1,0] = F_{SYS}/4,$
 $[0,1,1] = F_{SYS}/8, [1,0,0] = F_{SYS}/16, [1,0,1] = F_{SYS}/32,$
 $[1,1,0] = F_{SYS}/64, [1,1,1] = F_{SYS}/128$
 If PWMM is set, maximum pre-scale ratio is $F_{SYS}/32$.
- PWMM : PWM Mode Select
 [0] : 8-bit PWM, [1] : 10-bit PWM
- PWMF : PWM Interrupt Flag. Cleared by S/W
- CLR_P0 : Counter Reset Enable. Cleared by H/W.
- RUN_P0 : Counter Start Enable.

✓ PWMDH (DDh) : PWM Duty Data High Register

| | | | | | | | |
|---|---|---|---|---|---|---------|---------|
| - | - | - | - | - | - | PWMDH.1 | PWMDH.0 |
|---|---|---|---|---|---|---------|---------|

R/W(0) R/W(0)

Appendix.6 ADC (Analog-to-Digital Converter)

◆ MiDAS2.2

■ **ADCON** (EFh) : ADC Control & ADC Result Low Register : Value[1:0]

| | | | | | | | |
|-------|--------|--------|------|---|------|------|------|
| AD_EN | AD_REQ | AD_END | ADCF | - | ADIV | SAR1 | SAR0 |
|-------|--------|--------|------|---|------|------|------|

R/W(0) R/W(0) R(1) R/W(0) R/W(0) R/W(0) R/W(0)

- ◆ AD_EN : ADC ready enable.
- ◆ AD_REQ : ADC start.
Cleared by H/W when AD_END goes to 1 from 0.
- ◆ AD_END : Current ADC status.
0 = ADC is running now.
- ◆ ADCF : ADC interrupt flag. Must be cleared by S/W.
- ◆ ADIV : ADC input clock select.
0 = System clock (F_{SYS}) / 2. (Default)
1 = PWM input clock (F_{PWM})
- ◆ SAR1, SAR0 : Low bits of ADC result value.

◆ MiDAS220

■ **ADCON** (EFh) : ADC Control & ADC Result Low Register : Value[1:0]

| | | | | | | | |
|-------|--------|--------|------|-------|-------|------|------|
| AD_EN | AD_REQ | AD_END | ADCF | ADIV1 | ADIV0 | SAR1 | SAR0 |
|-------|--------|--------|------|-------|-------|------|------|

R/W(0) R/W(0) R(1) R/W(0) R/W(0) R/W(0) R/W(0) R/W(0)

- ◆ AD_EN : ADC ready enable.
- ◆ AD_REQ : ADC start.
Cleared by H/W when AD_END goes to 1 from 0.
- ◆ AD_END : Current ADC status.
0 = ADC is running now.
- ◆ ADCF : ADC interrupt flag. Must be cleared by S/W.
- ◆ ADIV1, ADIV0 : ADC input clock select.
[0,0] = System clock (F_{SYS}) / 2 (Default)
[0,1] = System clock (F_{SYS}) / 4
[1,0] = System clock (F_{SYS}) / 8
[1,1] = System clock (F_{SYS})
- ◆ SAR1, SAR0 : Low bits of ADC result value.

Appendix.7 I2C1

◆ MiDAS2.2

✓ I2CCFG1 (CCh) : I²C Configuration Register

| | | | | | | | |
|---|---|---|---|---|--------|--------|--------|
| - | - | - | - | - | ADSEL | SP_IE | GCE |
| - | - | - | - | - | R/W(0) | R/W(0) | R/W(0) |

- ADSEL : 7-bit / 10-bit Address Mode Selection in Slave mode
[0] : 7-bit mode [1] : 10-bit mode
- SP_IE : Start/Stop Interrupt Enable
[0] : Start/Stop Interrupt Disable [1] : Start/Stop Interrupt Enable
- GCE : General Call Enable in Slave mode
[1] : Respond to the general call address (0x00)

◆ MiDAS220

✓ I2CCFG1 (CCh) : I²C Configuration Register

| | | | | | | | |
|---|---|--------|--------|---|--------|--------|--------|
| - | - | DISHD | TXDBE | - | ADSEL | SP_IE | GCE |
| | | R/W(0) | R/W(0) | | R/W(0) | R/W(0) | R/W(0) |

- DISHD : Disable the function of SCLHD flag.
- XDBE : TX Double Buffer Enable
- ADSEL : 7-bit / 10-bit Address Mode Selection in Slave mode
[0] : 7-bit mode [1] : 10-bit mode
- SP_IE : Start/Stop Interrupt Enable
[0] : Start/Stop Interrupt Disable [1] : Start/Stop Interrupt Enable
- GCE : General Call Enable in Slave mode
[1] : Respond to the general call address (0x00)


✓ I2CSTH1 (C9h) : I²C Status High Register

| | | | | | | | |
|---|---|---|---|---|---|--------|-------|
| - | - | - | - | - | - | DBVLID | I2CBB |
| | | | | | | R(0) | R(0) |

- DBVLID : Valid flag of the double buffer.
This flag is set when user write to the TX buffer and cleared when the value is loaded to the shift buffer.
- I2CBB : I²C byte transmission busy flag
[0] : Not busy [1] : Busy

Appendix.8 Interrupt

◆ MiDAS2.2




A vertical pink arrow pointing upwards, labeled 'HIGH' at the top and 'LOW' at the bottom, with the word 'PRIORITY' written vertically along its shaft.

| Interrupt Sources | Address | Priority Level |
|-------------------|---------|----------------|
| LVD | 0033h | Highest |
| INT0 | 0003h | 2 Levels |
| TF0 | 000Bh | 2 Levels |
| INT1 | 0013h | 2 Levels |
| TF1 | 001Bh | 2 Levels |
| RI+TI | 0023h | 2 Levels |
| ADC | 003Bh | 2 Levels |
| INT2 | 0043h | 2 Levels |
| INT3 | 004Bh | 2 Levels |
| I2C0 | 0053h | 2 Levels |
| I2C1 | 005Bh | 2 Levels |
| WDT | 0063h | 2 Levels |
| PWM | 006Bh | 2 Levels |

NMI

◆ MiDAS220



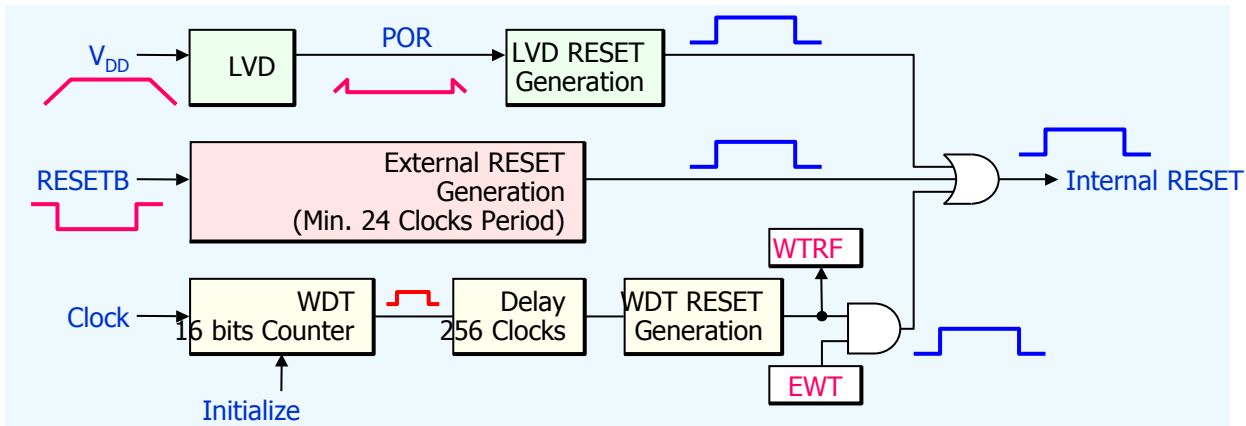
A vertical pink arrow pointing upwards, labeled 'HIGH' at the top and 'LOW' at the bottom, with the word 'PRIORITY' written vertically along its shaft.

| Interrupt Sources | Address | Priority Level |
|-------------------|---------|----------------|
| LVD | 0033h | Highest |
| INT0 | 0003h | 2 Levels |
| TF0 | 000Bh | 2 Levels |
| INT1 | 0013h | 2 Levels |
| TF1 | 001Bh | 2 Levels |
| RI+TI | 0023h | 2 Levels |
| ADC | 003Bh | 2 Levels |
| INT2 | 0043h | 2 Levels |
| INT3 | 004Bh | 2 Levels |
| I2C1 | 005Bh | 2 Levels |
| WDT | 0063h | 2 Levels |
| PWM | 006Bh | 2 Levels |

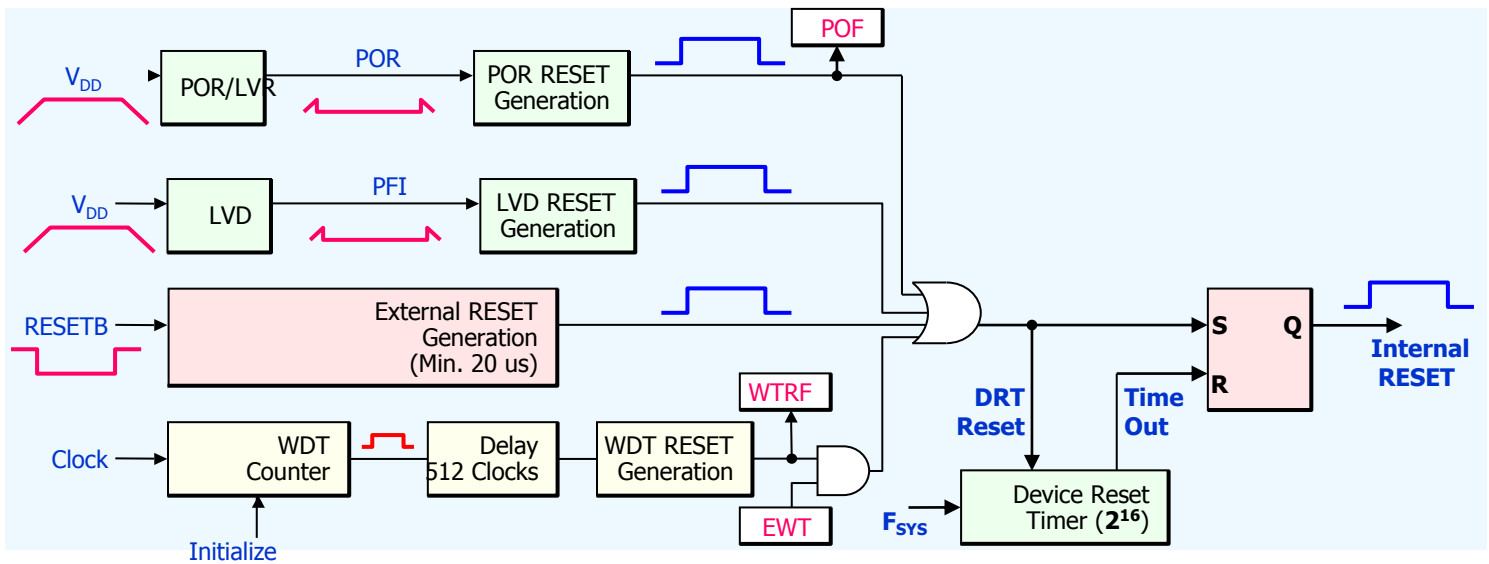
NMI

Appendix.9 Reset Circuit

◆ MiDAS2.2



◆ MiDAS230 /MiDAS220



Appendix.10 Clock Circuit

◆ MiDAS2.2

■ EXIF (91h) : External Interrupt Flag Register

| | | | | | | | |
|---|------|-----|-----|-------|------|------|-----|
| - | RTRG | IE3 | IE2 | XT/RG | RGMD | RGSL | BGS |
|---|------|-----|-----|-------|------|------|-----|

R/W(1) R/W(0) R/W(0) R/W(0) R(1) R/W(0) R/W(1)

- ◆ RT/RG : Internal RING clock selection [1] : 4MHz [0] : 32KHz
If the flag is switched,
RING 4MHz & RING 32KHz are switched into each other.
- ◆ RGSL : Ring select bit when power-down wake-up.
1 = When wake-up from power-down mode in XTAL
clock, use Ring oscillator as system clock during 65,536
XTAL clocks.

◆ MiDAS220

■ EXIF (91h) : External Interrupt Flag Register

| | | | | | | | |
|---|---|-----|-----|-------|------|------|-----|
| - | - | IE3 | IE2 | XT/RG | RGMD | RGSL | BGS |
|---|---|-----|-----|-------|------|------|-----|

R/W(0) R/W(0) R/W(0) R(1) R(1) R/W(1)

- ◆ RGSL : Ring select bit when power-down wake-up.
When wake-up from power-down mode in XTAL clock,
use RCLK as system clock during 65,536 RCLK cycles.
This bit is always 1.

| Control Flag | | | | | | | System Clock | Status Bit | | |
|--------------|-------|-------|-------|--------|--------|------|--|------------|------|------|
| RT/RG | XT/RG | RTOFF | XTOFF | RINGON | RINGON | RGSL | | RGMD | XTUP | RTUP |
| x | 1 | x | 0 | x | X | X | Crystal OSC. | 0 | 1 | 0/1 |
| 1 | 0 | x | X | x | 1 | X | Ring OSC. | 1 | 0/1 | 0/1 |
| 0 | 0 | x | x | 1 | X | x | Ring OSC(32KHz). | 0 | 1 | 0/1 |
| x | 1 | x | 0 | x | x | 0 | Crystal OSC. (during Power-down Wake-up) | 0 | 0 | 0/1 |
| 1 | 0 | x | x | x | 1 | 1 | Ring OSC. (during Power-down Wake-up) | 1 | 0 | 0/1 |
| 0 | 0 | x | x | 1 | X | 1 | Ring OSC(32KHz). (during Power-down Wake-up) | 0 | 0 | 0 |

| Control Flag | | | System Clock | Status Bit | |
|--------------|-------|--------|---|------------|------|
| XT/RG | XTOFF | RINGON | | RGMD | XTUP |
| 1 | 0 | X | Crystal OSC. | 0 | 1 |
| 1 | 0 | X | Precision OSC. (wake-up from power-down) | 1 | 0 |
| 0 | X | 1 | Precision OSC. | 1 | 0/1 |

Appendix.10 Clock Circuit (cont'd)

◆ MiDAS2.2

■ OSCICN (BEh) : Internal Ring Oscillator Control Register

| | | | | | | | |
|---|---|---|---|------|--------|------|------|
| - | - | - | - | DIV2 | RINGON | DIV1 | DIV0 |
|---|---|---|---|------|--------|------|------|

R/W(0) R/W(1) R/W(0) R/W(0)

- ◆ RINGON : 1 = Internal ring oscillator(24MHz) is running.
0 = Internal ring oscillator is killed.
Don't clear RINGON bit when XTRG = 0.
- ◆ DIV2, DIV1, DIV0 : Ring oscillator divider.
[0,0,0] = 4MHz ; Default
[0,0,1] = 2MHz
[0,1,0] = 1MHz
[0,1,1] = 0.5MHz
[1,0,0] = reserved
[1,0,1] = 12MHz
[1,1,0] = 6MHz
[1,1,1] = 3MHz

■ OSC2ICN (BFh) : Internal Ring2 Oscillator Control Register

| | | | | | | | |
|---|---|---|---|---|---|-------------|---------|
| - | - | - | - | - | - | OSC_REF_SEL | RING2ON |
|---|---|---|---|---|---|-------------|---------|

R/W(0) R/W(1)

- ◆ RING2ON: 1 = Internal ring oscillator(32KHz) is running.
0 = Internal ring oscillator is killed.
Don't clear RINGON bit when XTRG = 0.
- ◆ OSC_REF_SEL : RING reference selection

◆ MiDAS230/MiDAS220

■ OSCICN (BEh) : Internal Oscillator Control Register

| | | | | | | | |
|---|---|---|---|------|--------|------|------|
| - | - | - | - | DIV2 | RINGON | DIV1 | DIV0 |
|---|---|---|---|------|--------|------|------|

R/W(0) R/W(1) R/W(0) R/W(0)

- ◆ RINGON : 1 = Internal Precision Oscillator(11 MHz) is running.
0 = Internal Precision Oscillator is killed.
Don't clear RINGON bit when XTRG = 0.
- ◆ DIV2, DIV1, DIV0 : Internal oscillator divider
[0,0,0] = 3.68 MHz = $F_{POSC} / 3$; Default
[0,0,1] = 1.84 MHz = $F_{POSC} / 6$
[0,1,0] = 922 KHz = $F_{POSC} / 12$
[0,1,1] = 461 KHz = $F_{POSC} / 24$
[1,0,0] = reserved
[1,0,1] = 11.06 MHz = F_{POSC}
[1,1,0] = 5.53 MHz = $F_{POSC} / 2$
[1,1,1] = 2.76 MHz = $F_{POSC} / 4$

✓ RINGCON(95h) : Internal Oscillator Frequency Tuning

| | | | | | | | |
|----|----|----|----|----|----|----|----|
| S7 | S6 | S5 | S4 | S3 | S2 | S1 | S0 |
|----|----|----|----|----|----|----|----|

R/W(1) R/W(0) R/W(0) R/W(0) R/W(0) R/W(0) R/W(0) R/W(0)

✓ OSCBIAS(96h) : Internal Oscillator Bias Current Tuning

| | | | | | | | |
|--------|--------|--------|--------|--------|--------|--------|--------|
| BIAS.7 | BIAS.6 | BIAS.5 | BIAS.4 | BIAS.3 | BIAS.2 | BIAS.1 | BIAS.0 |
|--------|--------|--------|--------|--------|--------|--------|--------|

R/W(0) R/W(1) R/W(0) R/W(1) R/W(1) R/W(1) R/W(1) R/W(1)

✓ OSCREF(97h) : Internal Oscillator Reference Tuning

| | | | | | | | |
|---|---|---|--------|--------|--------|--------|--------|
| - | - | - | OREF.4 | OREF.3 | OREF.2 | OREF.1 | OREF.0 |
|---|---|---|--------|--------|--------|--------|--------|

R/W(1) R/W(0) R/W(1) R/W(1) R/W(1)

Final Comment

- ◆ The contents in this note is provided for quick reference.
- ◆ Please refer to the manuals of MiDAS220 and MiDAS2.2 for detailed descriptions.

Thank you !!!

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