AN

ChargerCore3.0 Application Guide for ChargerCore2.0 Users

V1.0

Dec. 6, 2011

1.1 Strong Points of ChargerCore3.0 vs. CC2.0

- Embedded FLASH with ISP (In System Programming)
  - ✓ The code memory of ChargerCore3.0 is FLASH memory, while that of ChargerCore2.0 is EPROM(OTP).
  - ✓ The embedded FLASH memory armed with ISP provides the maximum flexibility to production and logistics system.
    - Easy stock management for the small quantity batch production
    - The repair of code write failure at production line
    - The change of final product by changing embedded firmware before shipment
    - Upgrade of firmware at the customer service center
- Embedded EEPROM with IAP (In Application Programming)
  - ✓ Critical data for the application system can be easily stored with IAP in non-volatile EEPROM memory while the application system is operating.
  - ✓ Data retention : More than 10 years
  - ✓ Endurance : More than 100,000 cycles
- Internal precision oscillator with factory calibration
  - ✓ Provides stable clock against the variation of temperature and power supply voltage.
  - ✓ Typical deviation is ±1 % and the maximum deviation is ±2 %.
- Configurable LVD (Low Voltage Detector) with factory calibration
  - ✓ The internal LVD provides reset or interrupt to MCU against abnormal power condition.
  - ✓ The configurable LVD voltage ranges from 2.1V to 2.7V.
  - ✓ The resolution of calibration is 0.1V, which yields the maximum error as ±0.05V.

1.2 ChargerCore3.0 vs. ChargerCore2.0

◆ Common Features

- ✓ ChargerCore3.0 inherits most of the ChargerCore2.0 features except a few differences.
- ✓ Most of the electrical characteristics are similar to each other.
- ✓ However, the migration feasibility should be tested with samples.

◆ List of Differences

Item	ChargerCore3.0	ChargerCore2.0
Code Memory	FLASH 2K Byte	EPROM 4K Byte
Program with ISP	More than 100,000 times	Only one time
Embedded EEPROM with IAP	128 Byte (Part of Code Memory)	Not Available
Internal Clock	Precision OSC (±2 %), Freq = 461KHz ~ 11MHz	Ring OSC (±15 %), Freq = 456KHz ~ 3.65MHz
Power on reset / LVD	POR (1.6V) and Configurable LVD (2.1V ~ 2.7V)	POR (2.3V)
I/O ports initialization time	Initialized asynchronously by POR.	Initialized by synchronous internal reset.
I/O ports pull-up	I_{OHP} = -49uA @V_{DD}=5V,Pull-up is off when reset.	I_{OHP} = -140uA @V_{DD}=5V, Pull-up is on when reset.
I/O ports drive strength	I_{OL} = 17mA @V_{DD}=5V, I_{OH} = -18mA @V_{DD}=5V	I_{OL} = 20mA @V_{DD}=5V, I_{OH} = -15mA @V_{DD}=5V
I/O ports, unique pins	P0.6 (Replaces P2.5 of CC2.0)	P2.5
WDT	Overflow count : 2^{19}, 2^{20}, 2^{21}, 2^{22}	Overflow count : 2^{16}, 2^{18}, 2^{20}, 2^{21}
ADC	Included clock divider, Max. divide ratio = 8	Share clock divider of PWM, Max. divide ratio = 128
Interrupt	External interrupt : INT0, INT1 SFR's for interrupt: IE, IP	External interrupt : INT0, INT1, INT2 SFR's for interrupt: IE, IP, EIE, EIP
Serial Communication	Not Available	1 UART
Reset	External reset hold time is min. 20 us. Once triggered, internal reset holds 18 ms.	External reset hold time is min. 24 clocks. Once triggered, internal reset holds several clocks.

1.3 Firmware Guide for ChargerCore3.0

◆ Initialization routines for ChargerCore3.0

```
// Read the calibration data for Precision
// Oscillator from OTP area.
void init_posc(void)
{
  DPH     = 0;
  DPL     = 2;          // Low  byte of the address
  IAPCON  = 0x0D;       // Read byte in OTP
  RINGCON = IAPDAT;     // Read result

  DPL    += 2;          // Increment the address
  IAPCON  = 0x0D;       // Read byte in OTP
  OSCBIAS = IAPDAT;     // Read result

  DPL    += 2;          // Increment the address
  IAPCON  = 0x0D;       // Read byte in OTP
  OSCREF  = IAPDAT;     // Read result
}
```

```
// If reset is required at the same level as
// ChargerCore2.0, use following routine
void init_lvd_reset(void)
{
  DPH     = 0;
  DPL     = 8;          // Data address
  IAPCON  = 0x0D;       // Read byte in OTP
  LVDCFG  = IAPDAT;     // Configuration for 2.4V
  LVDCFG -= 1;          // Configuration for 2.3V
  LVDCFG |= 0x80;       // Enable LVD Reset
}
```

◆ Interrupt routines for ChargerCore3.0

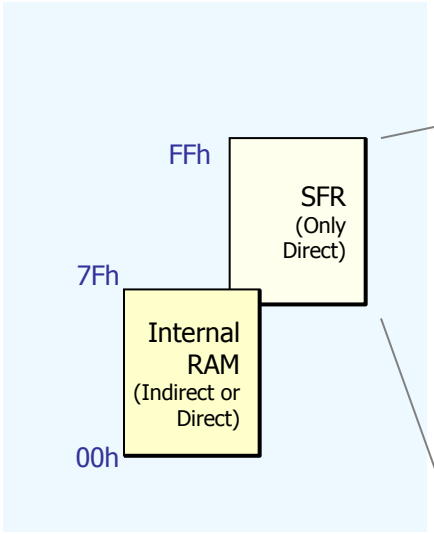
- ✓ One of major difference between ChargerCore3.0 and ChargerCore2.0 is the interrupt control for PWM and WDT due to the elimination of EIE and EIP.
- ✓ If the firmware is developed in C language, it is possible to write a compatible source for both MCU's.
- ✓ The rule : Set or clear individual bits (EPWM, EWDT, EADC, ET1, etc.) instead of writing the whole SFR's (IE, IP, EIE, or EIP).

```
// Example of a compatible C source
// Use proper header file for ChargerCore2.0
// or ChargerCore3.0

#include <ChargerCore20.H>
//#include <ChargerCore30.H>
void main()
{
            EPWM = 1;
            PPWM = 0;
            EA = 1;
            // Do something
            while(1);
}
void pwm_int() interrupt PWM_VECTOR
{
}
```

Appendix.1 SFR (Special Function Register) Map

SFR	: Common basic 8051 SFR
SFR	: Common SFR in ChargerCore3.0 and ChargerCore2.0 Family
SFR	: Unique SFR in ChargerCore2.0 Family
SFR	: Unique SFR in ChargerCore3.0 Family
	: Reserved for future use.



Bit addressable

F8h	**EIP**				**IAPWEN**	**IAPCON**	**IAPDAT**		FFh
F0h	B				**P0DIR**	**P1DIR**	**P2DIR**		F7h
E8h	**EIE**						**ADCR**	**ADCON**	EFh
E0h	ACC	**ADCSELH**	**ADCSEL**	**ALTSEL**	**P0SEL**	**P1SEL**	**P2SEL**		E7h
D8h	**WDCON**				**PWMCON**		**PWMD**		DFh
D0h	PSW				**P0TYPE**	**P1TYPE**	**P2TYPE**		D7h
C8h									CFh
C0h					**PMR**	**STATUS**	**LVDCFG**		C7h
B8h	IP						**OSCICN**		BFh
B0h									B7h
A8h	IE								AFh
A0h	P2								A7h
98h	**SCON**	**SBUF**							9Fh
90h	P1	**EXIF**				**RINGCON**	**OSCBIAS**	**OSCREF**	97h
88h	TCON	TMOD	TL0	TL1	TH0	TH1			8Fh
80h	P0	SP	DPL	DPH				PCON	87h

Appendix.2 I/O Ports

ChargerCore2.0

✓ P0SEL (E4h) : Port 0 Pull-up Control Register

-	-	P0SEL.5	P0SEL.4	-	P0SEL.2	P0SEL.1	P0SEL.0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

- 0 = Pull-up resistor ON (Default)
- 1 = Pull-up resistor OFF when ADC_EN (ADCON[7]) = 1

✓ P1SEL (E5h) : Port 1 Pull-up Control Register

-	-	-	-	-	-	P1SEL.1	P1SEL.0
						R/W(1)	R/W(1)

- 0 = Pull-up resistor ON
- 1 = Pull-up resistor OFF (Default)

✓ P2SEL (E6h) : Port 2 Pull-up Control Register

-	-	P2SEL.5	P2SEL.4	P2SEL.3	P2SEL.2	-	-
	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

- 0 = Pull-up resistor ON
- 1 = Pull-up resistor OFF when ADC_EN(ADCON[3]) = 1.

ChargerCore3.0

✓ P0SEL (E4h) : Port 0 Pull-up Control Register

-	P0SEL.6	P0SEL.5	P0SEL.4	-	P0SEL.2	P0SEL.1	P0SEL.0
R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(0)	R/W(0)

- 0 = Pull-up resistor ON / 1 = Pull-up resistor OFF

✓ P1SEL (E5h) : Port 1 Pull-up Control Register

-	-	-	-	-	P1SEL.2	P1SEL.1	P1SEL.0
					R/W(0)	R/W(1)	R/W(1)

- 0 = Pull-up resistor ON / 1 = Pull-up resistor OFF

✓ P2SEL (E6h) : Port 2 Pull-up Control Register

-	-	-	P2SEL.4	P2SEL.3	P2SEL.2	-	-
R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)

- 0 = Pull-up resistor ON / 1 = Pull-up resistor OFF (Default)

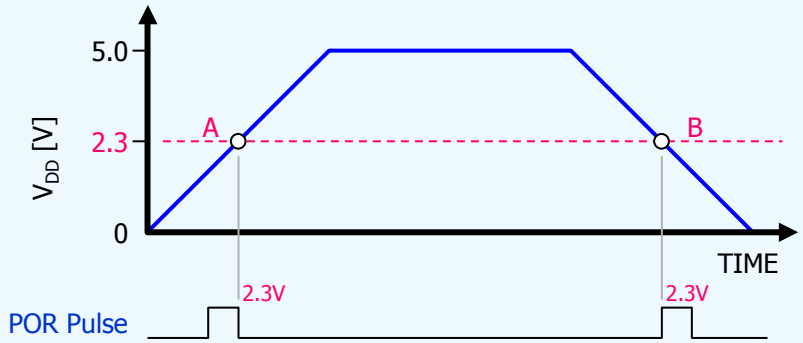
Appendix.3 POR / LVD

ChargerCore2.0

✓ PCON (87h) : Power Control Register

SMOD1	-	-	POF	GF1	GF0	PD	IDL
R/W(0)			R/W(1)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

- POF : Power Off flag. When power-on, POF = 1 by H/W.
- PD : Power-down mode bit



ChargerCore3.0

✓ LVDCFG (C6h) : LVD Configuration Register

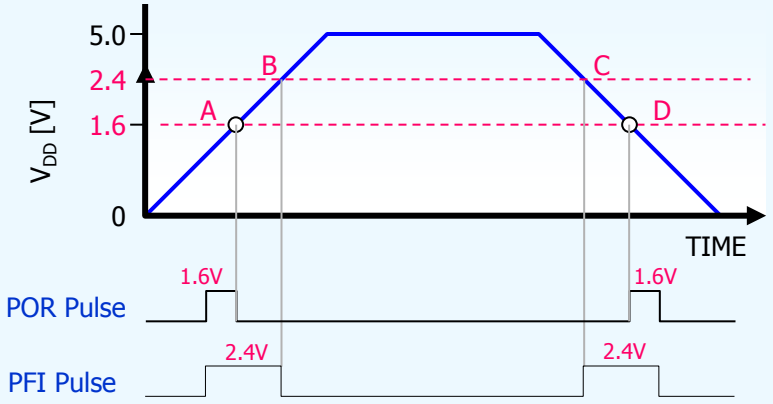
EPFR	EPFI	PFI	CFG4	CFG3	CFG2	CFG1	CFG0
R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R(1)	R/W(0)	R/W(1)

- EPFR : Power-fail reset enable.
- EPFI : Power-fail interrupt enable.
- PFI : Power-fail interrupt flag.
- CFG[4:0] : LVD Voltage Configuration

✓ PCON (87h) : Power Control Register

-	-	-	POF	GF1	GF0	PD	IDL
			R/W(1)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

- POF : Power off flag.
  When power-on, this flag bit will be set by H/W.
- PD : Power-down (Stop) mode enable.



Appendix.4 WDT (Watch Dog Timer)

ChargerCore2.0

✓ WDCON (D8h) : Watchdog Timer Control Register

WD1	WD0	-	-	WDIF	WTRF	EWT	RWT
R/W(1)	R/W(1)	R/W(0)	R/W(1)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

- WD[1:0] : WDT Clock Divide(1/4/8/32)
- WDIF : Watchdog Timer Interrupt Flag
- WTRF : Watchdog Timer Reset Flag. Only cleared by S/W.
- EWT : Watchdog Timer Reset Enable
- RWT : Restart Watchdog Timer

WD1	WD0	Interrupt Time-out (@4MHz)		Reset Time-out
0	0	$1x2^{16}$ clocks	16.38 ms	$1x2^{16}$ + 256 clocks
0	1	$4x2^{16}$ clocks	65.54 ms	$4x2^{16}$ + 256 clocks
1	0	$16x2^{16}$ clocks	262.14 ms	$16x2^{16}$ + 256 clocks
1	1	$32x2^{16}$ clocks	524.29 ms	$32x2^{16}$ + 256 clocks

ChargerCore3.0

✓ WDCON (D8h) : Watchdog Timer & Power Status Register

WD1	WD0	WDM	-	WDIF	WTRF	EWT	RWT
R/W(1)	R/W(1)	R/W(0)	R(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

- WD[1:0] : WDT Clock Divide
- WDM : Watchdog clock divide mode for Test (Do not set this bit in the application.)
- WDIF : Watchdog Timer Interrupt Flag
- WTRF : Watchdog Timer Reset Flag
- EWT : Watchdog Timer Reset Enable
- RWT : Restart Watchdog Timer

WD1	WD0	Interrupt Time-out (@ 4MHz)		Reset Time-out
0	0	2^{19} clocks	131 ms	2^{19} + 512 clocks
0	1	2^{20} clocks	262 ms	2^{20} + 512 clocks
1	0	2^{21} clocks	524 ms	2^{21} + 512 clocks
1	1	2^{22} clocks	1048 ms	2^{22} + 512 clocks

Appendix.5 ADC (Analog-to-Digital Converter)

◆ ChargerCore2.0

■ **ADCON** (EFh) : ADC Control & ADC Result Low Register : Value[1:0]

AD_EN	AD_REQ	AD_END	ADCF	AVREF	ADIV	SAR1	SAR0
R/W(0)	R/W(0)	R(1)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

- AD_EN : ADC ready enable.
- AD_REQ : ADC start.
  Cleared by H/W when AD_END goes to 1 from 0.
- AD_END : Current ADC status.
  0 = ADC is running now.
- ADCF : ADC interrupt flag. Must be cleared by S/W.
- AVREF : 1 = ADC reference voltage enable from P0.4.
- ADIV : ADC input clock select
  0 = System clock (F_{OSC}) / 2. (Default)
  1 = PWM input clock (F_{PWM})
- SAR1, SAR0 : Low bits of ADC result value.

◆ ChargerCore3.0

■ **ADCON** (EFh) : ADC Control & ADC Result Low Register : Value[1:0]

AD_EN	AD_REQ	AD_END	ADCF	ADIV1	ADIV0	SAR1	SAR0
R/W(0)	R/W(0)	R(1)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

- AD_EN : ADC ready enable.
- AD_REQ : ADC start.
  Cleared by H/W when AD_END goes to 1 from 0.
- AD_END : Current ADC status.
  0 = ADC is running now.
- ADCF : ADC interrupt flag. Must be cleared by S/W.
- ADIV1, ADIV0 : ADC input clock select.
  [0,0] = System clock (F_{SYS}) / 2 (Default)
  [0,1] = System clock (F_{SYS}) / 4
  [1,0] = System clock (F_{SYS}) / 8
  [1,1] = System clock (F_{SYS})
- SAR1, SAR0 : Low bits of ADC result value.

Appendix.6 Interrupt

◆ ChargerCore2.0

HIGH

PRIORITY

Interrupt Sources	Address	Priority Level
$\overline{INT0}$	0003h	2 Levels
TF0	000Bh	2 Levels
$\overline{INT1}$	0013h	2 Levels
TF1	001Bh	2 Levels
RI+TI	0023h	2 Levels
ADC	003Bh	2 Levels
INT2	0043h	2 Levels
	004Bh	2 Levels
WDT	0063h	2 Levels
PWM	006Bh	2 Levels

* Interrupt related to SFR (refer to Appendix B : SFR Description)

✓ TCON (88h)

TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0

✓ EXIF (91h)

-	-	IE3	IE2	XT/RG	RGMD	RGSL	BGS

✓ IE (A8h)

EA	EADC	-	ES	ET1	EX1	ET0	EX0

✓ IP (B8h)

-	PADC	-	PS	PT1	PX1	PT0	PX0

✓ EIE (E8h)

-	-	EPWM	EWDT	-	-		EX2

✓ EIP (F8h)

-		PPWM	PWDT	-	-		PX2

✓ WDCON (D8h)

WD1	WD0	-	-	WDIF	WTRF	EWT	RWT

✓ PWMCON (DCh)

P0SEL	PS2_P0	PS1_P0	PS0_P0	-	PWMF	CLR_P0	RUN_P0

◆ ChargerCore3.0

HIGH

PRIORITY

LOW

Interrupt Sources	Address	Priority Level
LVD	0033h	NMI
INT0B	0003h	2 Levels
TF0	000Bh	2 Levels
INT1B	0013h	2 Levels
TF1	001Bh	2 Levels
WDT	0023h	2 Levels
PWM	002Bh	2 Levels
ADC	003Bh	2 Levels

✓ TCON (88h)

TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0

✓ IE (A8h)

EA	EADC	EPWM	EWDT	ET1	EX1	ET0	EX0

✓ IP (B8h)

-	PADC	PPWM	PWDT	PT1	PX1	PT0	PX0

✓ LVDCFG (C6h)

EPFR	EPFI	PFI	CFG4	CFG3	CFG2	CFG1	CFG0

✓ WDCON (D8h)

WD1	WD0	WDM	-	WDIF	WTRF	EWT	RWT

✓ PWMCON (DCh)

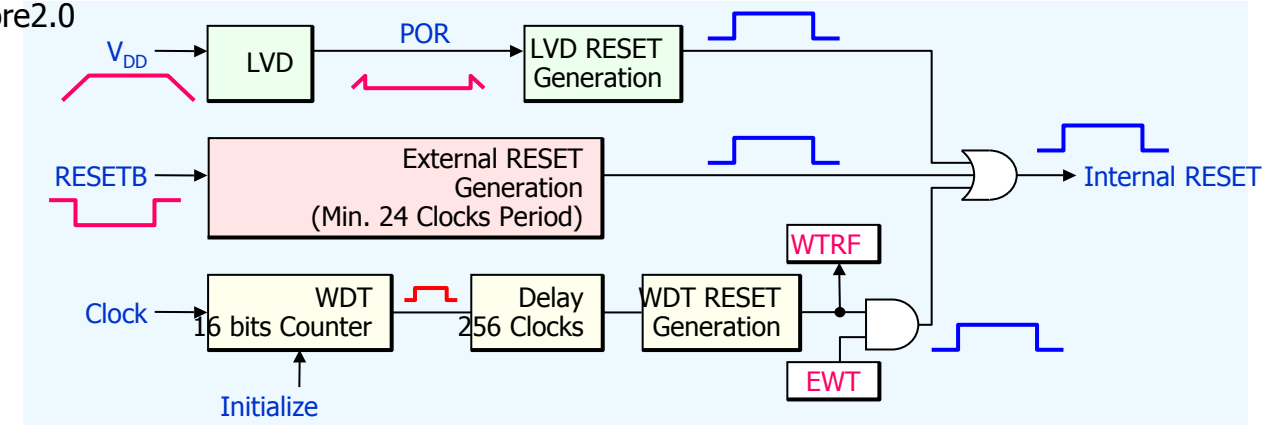
PWM06	PS2_P0	PS1_P0	PS0_P0	-	PWMF	CLR_P0	RUN_P0

✓ ADCON (EFh)

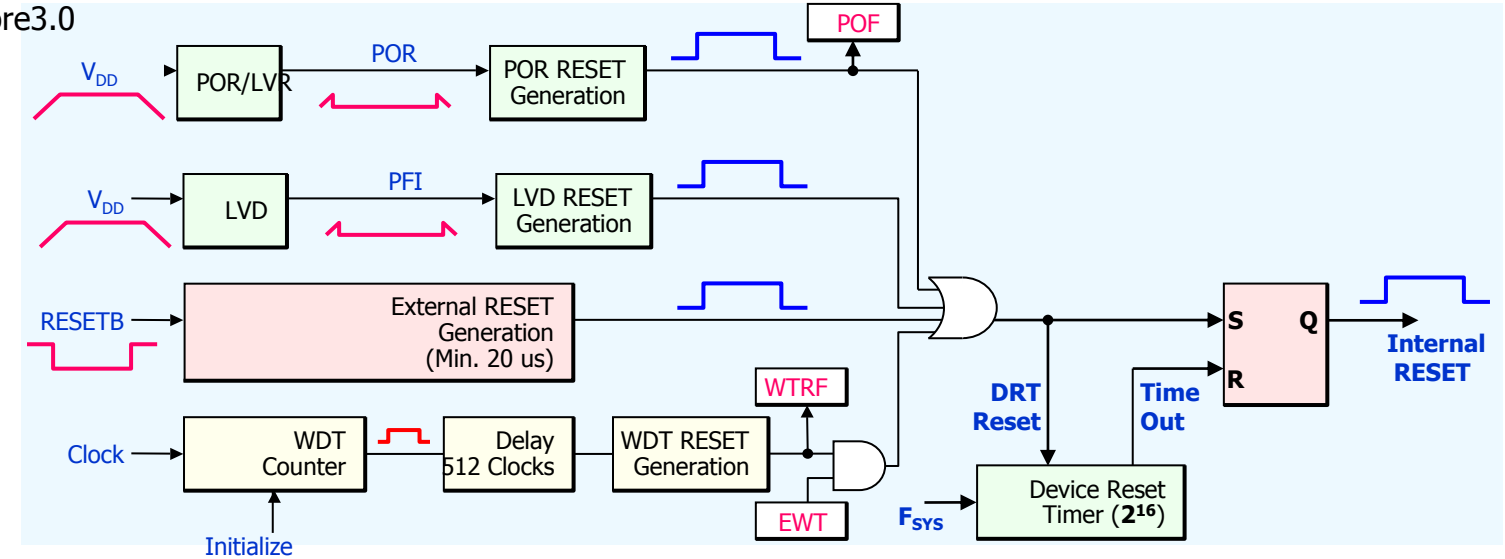
AD_EN	AD_REQ	AD_END	ADCF	ADIV1	ADIV0	SAR1	SAR0

Appendix.7 Reset Circuit

- ChargerCore2.0



- ChargerCore3.0



Appendix.8 Clock Circuit

◆ ChargerCore2.0

■ **EXIF** (91h) : External Interrupt Flag Register

-	-	-	IE2	XT/RG	RGMD	RGSL	BGS
		R/W(0)	R/W(0)	R/W(0)	R(1)	R/W(0)	R/W(1)

- ◆ IE2 : External interrupt 2 flag. Cleared by S/W.
- ◆ XT/RG : System clock selection
  0 = Internal Ring oscillator is selected as system clock.
  1 = External clock is selected as system clock.
- ◆ RGMD : Ring mode. Now system clock is Ring or XTAL.
  Generally RGMD is the invert of XT/RG.
- ◆ RGSL : Ring select bit when power-down wake-up.
  1 = When wake-up from power-down mode in XTAL clock, use Ring oscillator as system clock during 65,536 XTAL clocks.
- ◆ BGS : Band-gap select. (Default = 1)
  0 = Band-gap block (LVD) will do not run in power-down mode, but function during normal mode.
  It will support the significant power savings in power-down mode.
  1 = Band-gap block (LVD) will run in power-down mode.

Control Flag				System Clock	Status Bit	
XT/RG	XTOFF	RINGON	RGSL		RGMD	XTUP
1	0	X	X	Crystal OSC.	0	1
0	X	1	X	Ring OSC.	1	0/1
1	0	X	0	Crystal OSC. (during Power-down Wake-up)	0	0
0	X	1	1	Ring OSC. (during Power-down Wake-up)	1	0

◆ ChargerCore3.0

■ **EXIF** (91h) : External Interrupt Flag Register

-				XT/RG	RGMD	RGSL	BGS
-				R/W(0)	R(1)	R(1)	R/W(1)

- ◆ XT/RG : System clock selection.
  0 = Internal Precision oscillator is selected as system clock.
  1 = External clock is selected as system clock.
- ◆ RGMD : RCLK mode. Now system clock is POSC or XTAL.
  Generally RGMD is the invert of XT/RG.
- ◆ RGSL : RCLK select bit when power-down wake-up.
  If set, when wake-up from power-down in XTAL clock, use RCLK as system clock during the first 65,536 cycles.
  This bit is always 1.
- ◆ BGS : Band-gap select. (Default = 1)
  If 0, Band-gap block (POR) will be off in power-down mode.
  If 1, Band-gap block (POR) will run in power-down mode.

Control Flag			System Clock	Status Bit	
XT/RG	XTOFF	RINGON		RGMD	XTUP
1	0	X	Crystal OSC.	0	1
1	0	X	Precision OSC. (wake-up from power-down)	1	0
0	X	1	Precision OSC.	1	0/1

Appendix.8 Clock Circuit (cont'd)

◆ ChargerCore2.0

■ **OSCICN** (BEh) : Internal Ring Oscillator Control Register

-	-	-	-	-	RINGON	DIV1	DIV0
					R/W(1)	R/W(0)	R/W(0)

◆ RINGON : 1 = Internal ring oscillator is running.
0 = Internal ring oscillator is killed.
Don't clear RINGON bit when XTRG = 0.

◆ DIV1, DIV0 : Ring oscillator divider.
[0,0] = 3.65MHz/1
[0,1] = 3.65MHz/2
[1,0] = 3.65MHz/4
[1,1] = 3.65Mhz/8

◆ ChargerCore3.0

■ **OSCICN** (BEh) : Internal Oscillator Control Register

-	-	-	-	DIV2	RINGON	DIV1	DIV0
				R/W(0)	R/W(1)	R/W(0)	R/W(0)

◆ RINGON : 1 = Internal Precision Oscillator(11 MHz) is running.
0 = Internal Precision Oscillator is killed.
Don't clear RINGON bit when XTRG = 0.

◆ DIV2, DIV1, DIV0 : Internal oscillator divider
[0,0,0] = 3.68 MHz = F_{POSC} / 3 ; Default
[0,0,1] = 1.84 MHz = F_{POSC} / 6
[0,1,0] = 922 KHz = F_{POSC} / 12
[0,1,1] = 461 KHz = F_{POSC} / 24
[1,0,0] = reserved
[1,0,1] = 11.06 MHz = F_{POSC}
[1,1,0] = 5.53 MHz = F_{POSC} / 2
[1,1,1] = 2.76 MHz = F_{POSC} / 4

✓ RINGCON(95h) : Internal Oscillator Frequency Tuning

S7	S6	S5	S4	S3	S2	S1	S0
R/W(1)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)	R/W(0)

✓ OSCBIAS(96h) : Internal Oscillator Bias Current Tuning

BIAS.7	BIAS.6	BIAS.5	BIAS.4	BIAS.3	BIAS.2	BIAS.1	BIAS.0
R/W(0)	R/W(1)	R/W(0)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)

✓ OSCREF(97h) : Internal Oscillator Reference Tuning

-	-	-	OREF.4	OREF.3	OREF.2	OREF.1	OREF.0
			R/W(1)	R/W(0)	R/W(1)	R/W(1)	R/W(1)

Final Comment

- The contents in this note is provided for quick reference.
- Please refer to the manuals of ChargerCore3.0 and ChargerCore2.0 for detailed descriptions.

Thank you !!!