CICore1.0

Common Interface Hardware Controller

for Set-Top-Box Application

Ver. 1.2

May 2012

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1. Product Overview

The CICORE1.0 controller is the hardware extension of the Industry Standard, SCM Microsystems' second generation Common Interface integration package. It enables CI Driver software to directly address two complete independent Common Interface modules.

As such, it contributes to offer an optimized, homogeneous and complete solution for digital TV receiver manufacturer that wants quickly to implement the Common Interface.

CICORE1.0 includes the necessary I/Os to interface the MPEG Transport stream generated by the receiver demodulator and to daisy chain it through two modules and back it to the de-multiplexer. Due to internal voltage level translators, no additional component is needed for voltage level translation.

CICORE1.0 interfaces with major digital TV receiver microprocessors. An I²C bus is used for initialization and module selection, while a Universal Control Signal Generator (UCSG) maps CPU control bus into Command Interface control signals. To minimize pin count, host address and data buses transit through external buffers that are driven by CICORE1.0.

CICORE1.0 includes a memory mode that allows software to use either of the two Common interface slots to read/write an 8-bit PC Card Memory card. This feature gives the receiver memory extension capability for software upgrade or better performance.

1.1 Glossary

DVB_CI:	Digital Video Broadcast – Common Interface
NRSS-B:	National Renewable Security Standard – PCMCIA
DAVIC:	Digital Audio Visual Council
PCMCIA:	Personal Computer Memory Card International Association
MPEG:	Moving Picture Experts Group
DEMUX:	Demultiplexer
PQFP:	Plastic Quad Flat Pack
Common interface:	The Common Interface is a technology which allows separation of conditional access functionality from a digital TV receiver-decoder (Host) into a removable conditional access module (CAM)
CAM:	Conditional access module
UCSG:	Control Signal Generator
I^2C:	Inter-Integrated Circuit

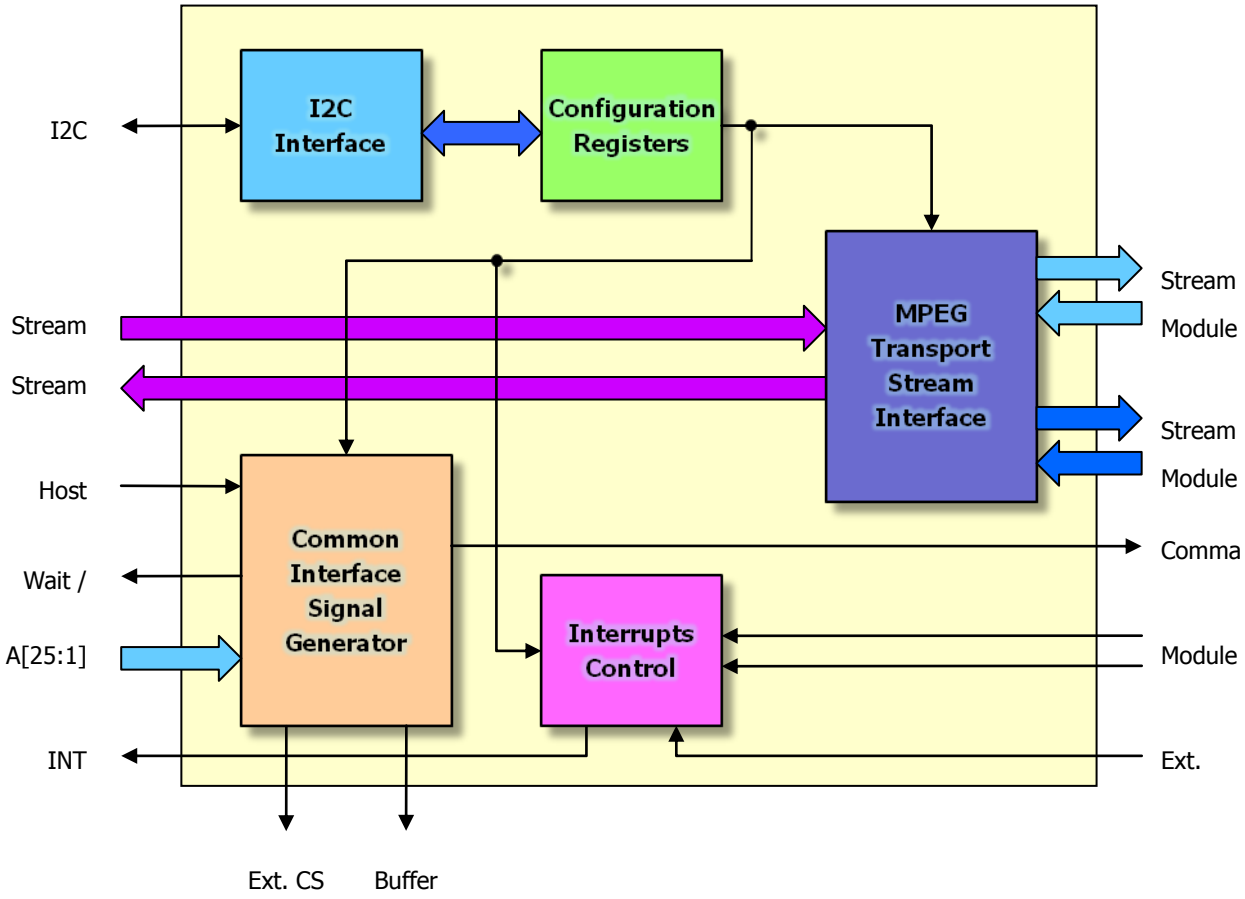
SDA:	Serial Data Line
SCL:	Serial Clock Line

2. Features

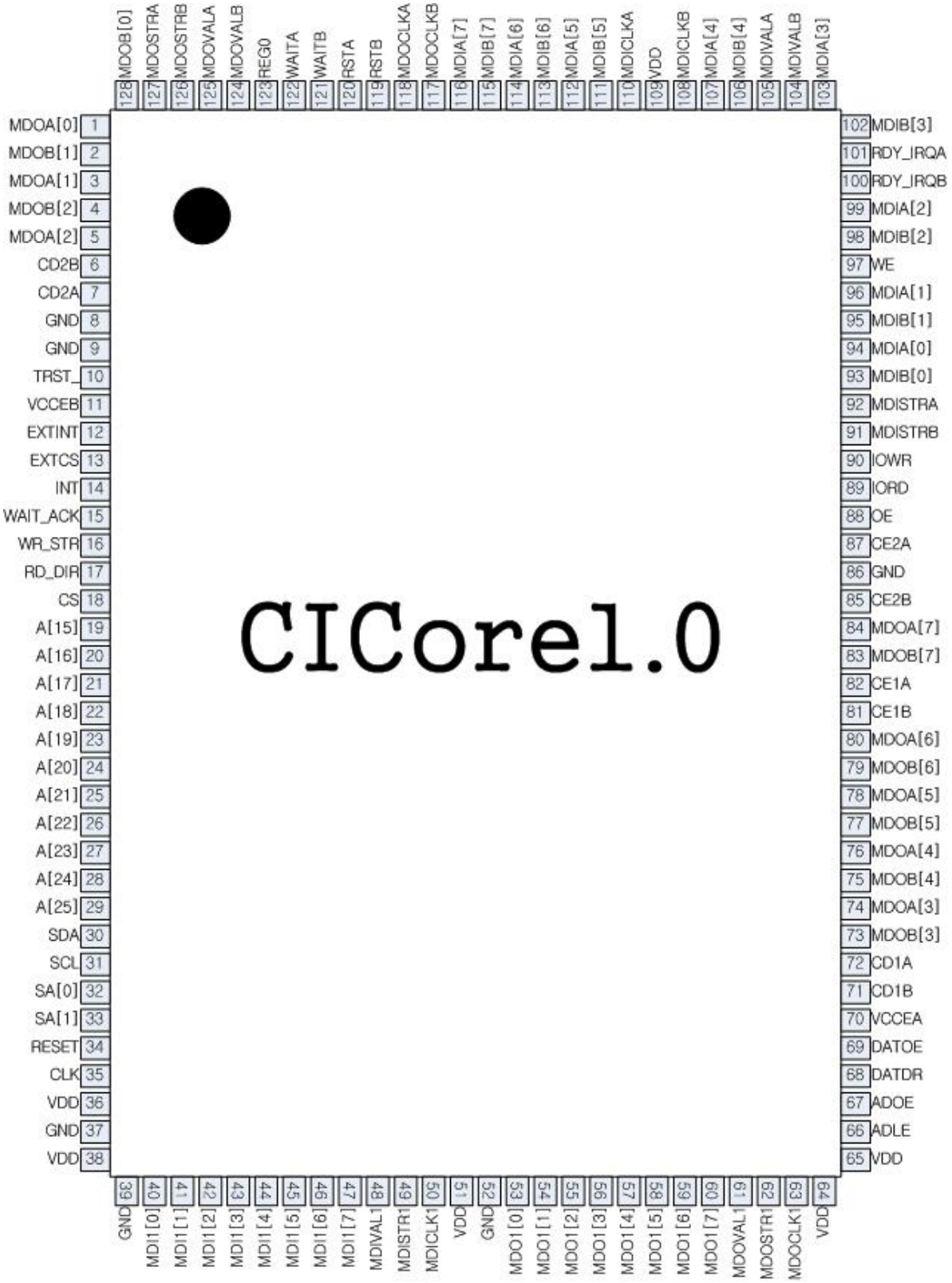
- Module Interface
  - 2 full independent module capability
  - Common Interface Standard compliant
    - DVB_CI (CENELEC EN-50221)
    - NRSS-B (SCTE IS-679 Part B)
    - DAVIC v1.2 (CA0 interface)
  - Memory PCMCIA compliance (R2)
    - 8-bit data access
    - 26-bit address Memory Card
  - Attribute Memory access (CIS, Tupple)
  - High speed capability
    - Up to 20Mbits/s on Command Interface
    - Up to 100Mbits/s on Transport Stream
  - Polling and Interrupt modes
  - Hot Insertion (Automatic and Reset VCC handling)
  - 3.3V or 5V I/O buffers
- PQFP 128 package
- Host microprocessor Interface
  - Universal Control Signal Generator (UCSG)
  - PC Card control signals generation
  - Supports PowerPC, ARM, ST20, 68xxx, TMS, LSI 64008, TC81220F, IDTR3041 host microprocessors
  - I^2C port
    - CICOR Set-up
    - Slot selection
  - Cascade mode management
  - Chip Select bank and Interrupt facilities
  - 3.3V or 5V I/O buffers
- Digital Video Stream Interface
  - MPEG II Transport Stream compliant
  - 3.3V or 5V I/O buffer for direct interface with FEC and DEMUX ICs

3. Block Diagram

In case of modules order is significant, CICORE1.0 may virtually swap them (SCM' Patent Pending) after identifying which module must be in front of the transport stream.



3. Pin Configuration



4. Pin Description

Signal	Package Number	Direction I/O	Descriptions
MODA[0]	1	I	MPEG data input 0 from module A
MDOB[1]	2	I	MPEG data input 1 from module B
MDOA[1]	3	I	MPEG data input 1 from module A
MDOB[2]	4	I	MPEG data input 2 from module B
MDOA[2]	5	I	MPEG data input 2 from module A
CD2B	6	I	Card detect signal 2 of module B
CD2A	7	I	Card detect signal 2 of module A
GND	8	power	ground
GND	9	power	ground
TRST_	10	I	Test Reset
VCCEB	11	O	VCC switch control signal of modules
EXTINT	12	I	Interrupt signal of external device
EXTCS	13	O	Chip select signal of external device
INT	14	O	Interrupt output to microprocessor
WAIT_ACK	15	O	Wait or acknowledge signal to microprocessor
WR_STR	16	I	Write or strobe signal from microprocessor
RD_DIR	17	I	Read or direction signal from microprocessor
CS	18	I	Chip select signal from microprocessor
A[15]	19	I	Address output bit 15of microprocessor
A[16]	20	I	Address output bit 16 of microprocessor
A[17]	21	I	Address output bit 17 of microprocessor
A[18]	22	I	Address output bit 18 of microprocessor
A[19]	23	I	Address output bit 19 of microprocessor
A[20]	24	I	Address output bit 20 of microprocessor
A[21]	25	I	Address output bit 21 of microprocessor
A[22]	26	I	Address output bit 22 of microprocessor
A[23]	27	I	Address output bit 23 of microprocessor
A[24]	28	I	Address output bit 24 of microprocessor
A[25]	29	I	Address output bit 25 of microprocessor
SDA	30	IO	I²C data

SCL	31	I	I²C clock
SA[0]	32	I	I²C address bit 0
SA[1]	33	I	I²C address bit 1
RESET	34	I	Synchronous Chip reset (Active high)
CLK	35	I	Clock input
VDD	36	power	
GND	37	power	
VDD	38	power	
GND	39	power	
MDI1[0]	40	I	MPEG data input 0
MDI1[1]	41	I	MPEG data input 1
MDI1[2]	42	I	MPEG data input 2
MDI1[3]	43	I	MPEG data input 3
MDI1[4]	44	I	MPEG data input 4
MDI1[5]	45	I	MPEG data input 5
MDI1[6]	46	I	MPEG data input 6
MDI1[7]	47	I	MPEG data input 7
MDIVAL1	48	I	MPEG data valid signal input
MDISTR1	49	I	MPEG data start signal input
MDICLK1	50	I	MPEG clock signal input
VDD	51	power	Power supply
GND	52	power	ground
MDO1[0]	53	O	MPEG data output 0
MDO1[1]	54	O	MPEG data output 1
MDO1[2]	55	O	MPEG data output 2
MDO1[3]	56	O	MPEG data output 3
MDO1[4]	57	O	MPEG data output 4
MDO1[5]	58	O	MPEG data output 5
MDO1[6]	59	O	MPEG data output 6
MDO1[7]	60	O	MPEG data output 7
MDOVAL1	61	O	MPEG data valid signal output
MDOSTR1	62	O	MPEG data start signal output
MDOCLK1	63	O	MPEG clock signal output
VDD	64	power	Power supply
VDD	65	power	Power supply

ADLE	66	O	External address buffer latch enable signal
ADOE	67	O	External address buffer output enable signal
DATDR	68	O	External data buffer direction
DATOE	69	O	External data buffer output enable
VCCEA	70	O	VCC switch control signal of modules
CD1B	71	I	Card detect signal 1 of module B
CD1A	72	I	Card detect signal 1 of module A
MDOB[3]	73	I	MPEG data input 3 from module B
MDOA[3]	74	I	MPEG data input 3 from module A
MDOB[4]	75	I	MPEG data input 4 from module B
MODA[4]	76	I	MPEG data input 4 from module A
MDOB[5]	77	I	MPEG data input 5 from module B
MDOA[5]	78	I	MPEG data input 5 from module A
MODB[6]	79	I	MPEG data input 6 from module B
MDOA[6]	80	I	MPEG data input 6 from module A
CE1B	81	O	Card enable signal 1 of module B
CE1A	82	O	Card enable signal 1 of module A
MODB[7]	83	I	MPEG data input 7 from module B
MODA[7]	84	I	MPEG data input 7 from module A
CE2B	85	O	Card enable signal 2 of module B
GND	86	power	ground
CE2A	87	O	Card enable signal 2 of module A
OE	88	O	Output enable signal to modules
IORD	89	O	I/O read signal tomodules
IOWR	90	O	I/O write signal to modules
MDISTRB	91	O	MPEG data start signal to module B
MDISTRA	92	O	MPEG data start signal to module A
MDIB[0]	93	O	MPEG data output 0 to module B
MDIA[0]	94	O	MPEG data output 0
MDIB[1]	95	O	MPEG data output 1 to module B
MDIA[1]	96	O	MPEG data output 1 to module A
WE	97	O	Write enable signal to modules
MDIB[2]	98	O	MPEG data output 2 to module B
MDIA[2]	99	O	MPEG data output 2 to module A
RDY_IRQB	100	I	RDY/IRQ signal from module B

RDY_IRQA	101	I	RDY/IRQ signal from module A
MDIB[3]	102	O	MPEG data output 3 to module B
MDIA[3]	103	O	MPEG data output 3
MDIVALB	104	O	MPEG data valid signal to module B
MDIVALA	105	O	MPEG data valid signal to module A
MDIB[4]	106	O	MPEG data output 4 to module B
MDIA[4]	107	O	MPEG data output 4 to module A
MDICLKB	108	O	MPEG clock signal to module B
VDD	109	power	Power supply
MDICLKA	110	O	MPEG clock signal to module A
MDIB[5]	111	O	MPEG data output 5 to module B
MDIA[5]	112	O	MPEG data output 5 to module A
MDIB[6]	113	O	MPEG data output 6 to module B
MDIA[6]	114	O	MPEG data output 6 to module A
MDIB[7]	115	O	MPEG data output 7 to module B
MDIA[7]	116	O	MPEG data output 7 to module A
MDOCLKB	117	I	MPEG clock signal from module B
MDOCLKA	118	I	MPEG clock signal from module A
RSTB	119	O	Reset of module B
RSTA	120	O	Reset of module A
WAITB	121	I	WAIT signal of module B
WAITA	122	I	WAIT signal of module A
REG	123	O	REG signal to modules
MDOVALB	124	I	MPEG data valid input from module B
MDOVALA	125	I	MPEG data valid input from module A
MDOSTRB	126	I	MPEG data start input from module B
MDOSTRA	127	I	MPEG data start input from module A
MDOB[0]	128	I	MPEG data input 0 to module B

5. Host Microprocessor Interface

5.1 Configuration Interface

CICORE1.0 needs a clock source at 27MHz frequency with a duty cycle comprised between 33% and 67%. This frequency is commonly available in any digital video system.

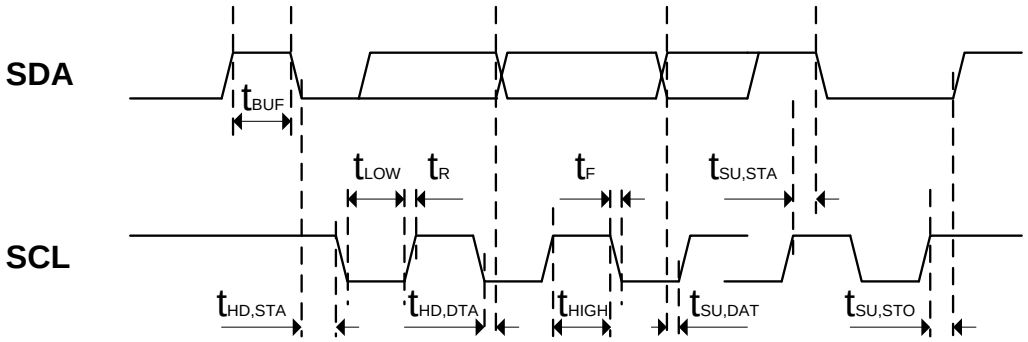
CICORE1.0 configuration is achieved by accessing the various registers through a standard I²C interface. The I²C device address can be chosen among four values by connecting SA1 and SA0 with VCC or GND.

The base address can be chosen between 80h, 82h, 84h or 86h allowing the connection of up to four CICORE1.0 on the same bus. Refer to I²C standard of Philips data book for the detailed AC/DC characteristics and the timing diagram of the I²C interface.

CICORE1.0 supports a bus control of various microprocessors. At reset, the host microprocessor interface is disabled –CS, RD/DIR and WR/STR inputs are inactive and WAIT/ACK and INT are in high impedance state. The only available access is the configuration interface(I²C) which permits to set up the CICORE1.0. Once the proper parameters have been entered in the CICORE1.0, the interface is enabled by setting the LOCK bit in the control register('h1F). The access to the modules is then possible and some parameters related to the host microprocessor interface are impossible to modify.

Host microprocessor input control signals are CS, RD/DIR, WR/STR and output signals are WAIT/ACK and INT. Input and output active levels can be individually set up by configuration bits. The output buffer structure is also configurable to be either open-drain or push-pull. CICORE1.0 inputs the RD/DIR, WR/STR and CICORE1.0 inputs the RD/DIR, WR/STR and CS signals from host microprocessor, WAITA and WAITB from the modules and generates all the control signals to modules, host microprocessor, buffers and external device : CE1A, CE2A, CE1B, CE2B, REG, OE, WE, IORD, IOWR, WAIT, ACK, ADLE, DATDIR, DATOE.

I²C bus interface



The I²C bus timing characteristics and bus-line capacitance are given in below table, and below figure shows the timing definitions for the I²C bus. The minimum HIGH and LOW periods of the SCL clock specified in below table determine the maximum bit transfer rates of 400kbits/sec for Fast-mode.

Symbol	Item	Min	Max	Unit
f_{scl}	SCL frequency		400	KHz
t_{BUF}	Bus free time between stop and start	1.3		μsec
$t_{HD,STA}$	Hold time start condition	0.3		μsec
t_{LOW}	SCL low period	1.3		μsec
t_{HIGH}	SCL high period	0.6		μsec
$t_{SU,STA}$	Setup time before a repeated start	0.6		μsec
$t_{HD,DAT}$	Data hold time	0	0.9	μsec
$t_{SU,DAT}$	Data setup time	100		nsec
t_R	Rise time for both SDA and SCL signals	20	300	nsec
t_F	Fall time for both SDA and SCL signals	20	300	nsec
$t_{SU,STO}$	Setup time before a stop condition	0.6		nsec
C_b	Capacitive load for each bus line		400	pF

5.2 Universal Microprocessor Control Signal Generator (UCSG)

CICORE1.0 can be connected to various CPUs, each of them having a different external bus control structure with different signals and timings. To interface with a large number of different microprocessors, the host microprocessor interface includes a fully configurable UCSG block that generates the right PCMCIA control signals.

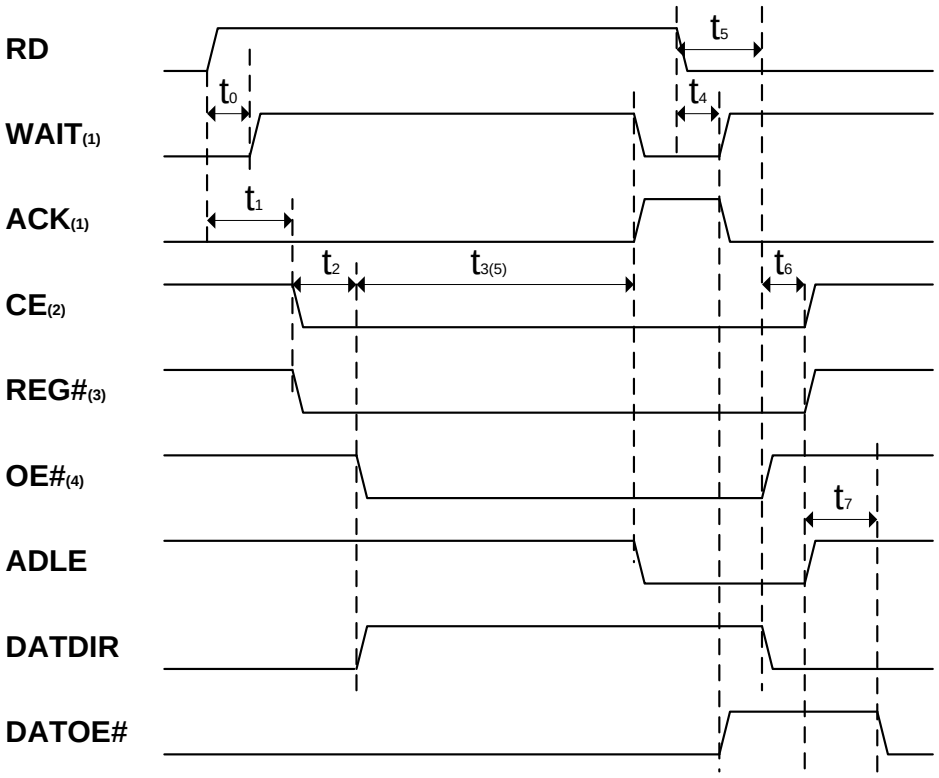
Host microprocessor input control signals are CS, RD/DIR, WR/STR and output signals are WAIT/ACK and INT. Input and output active levels can be individually set up by configuration bits, and the output buffer structure is also configurable to be either open-drain or push-pull in the UCSG1 and UCSG2 registers.

- CS: Chip select signal indicates to the CICORE1.0 that the current bus cycle is addressed to one of the modules (or external device)
- RD/DIR: Read strobe or direction signal. This signal function can be chosen with the RDIR bit. Read strobe indicates a valid read bus cycle or direction signal indicates the bus transfer direction when a valid bus transfer is indicated by the transfer strobe signal
- WR/STR: Write strobe or transfer strobe. This signal function can be adjusted with the WSTR bit. Write strobe indicates a valid write bus cycle or transfer strobe indicates a valid bus transfer in direction indicated by RD/DIR state.
- WAIT/ACK: Wait or Acknowledge transfer. In WAIT mode, this signal inserts wait cycles in the bus read or write operation in process. In ACK mode, this signal indicates the completion of the bus cycle.
- INT: Interrupt output to the host microprocessor.

The UCSG (universal control signals generator) inputs the RD / DIR, WR / STR and CS signals from host microprocessor, WAITA# and WAITB# from the modules and generates all the control signals to modules, host microprocessor, buffers and external device : CE1A#, CE2A#, CE1B#, CE2B#, REG#, OE#, WE#, IORD#, IOWR#, WAIT, ACK, ADLE, ADOE#, DATDIR, DATOE#.

The INT output to the microprocessor can be configured to be active high or low and driven by a push-pull or open-drain. Interrupts are managed by CICORE1.0 and one output is available for connection CICORE1.0 to the microprocessor interrupt controller. Five interrupt sources are available: two modules detection, two modules IRQ, and one external device interrupt. Modules detection interrupts are latched inside the CICORE1.0 and are acknowledged on the reading of the Interrupt Status Register. Each interrupt source can be individually masked. When masked, an incoming interrupt is visible in the Interrupt Status Register but does not generate an interrupt to the host microprocessor.

5.3 Read Access



Notes

(1) The WAIT/ACK output is either WAIT or ACK formatted according to the WAIT/ACK pin settings (driving structure, active level)

(2) Depending on the read access type, CE can be either CE1A# or CE1B# for access to memory or IO mode to module A or B, CE2A# or CE2B# for access in EC(Extended Channel) mode, or even EXTCS for access to external device in regenerate mode.

(3) REG# signal is not asserted during a common memory or external access.

(4) OE# signal is asserted during a memory access(attribute or common). It is replaced by IORD# during an IO read cycle, an EC read cycle, or an external device in regenerate mode.

(5) t3 can be lengthened by the insertion of wait cycles. When the module asserts WAIT# signal, t3 cycles counter stops until WAIT# becomes inactive anew.

Memory read timings are given for various cycle durations. In attribute memory mode, only 600 nsec and 300 nsec cycles are available. In common memory mode, 300 n sec doesn't exist. IO and external device in regenerate mode share the same timing specifications as they all use IORD# and IOWR# signals. Timings are given in CICORE1.0 clock cycles. They are calculated to comply with PCMCIA specifications when 27 MHz

clock is used.

*unit : ns(cycle)

	Memory read						IO, EC, EXT
	600	300	250	200	150	100	
t0 max	15						
t1 max	74(2)						
t2	111(3)	37(1)	37(1)	37(1)	37(1)	37(1)	74(2)
t3	518(14)	296(8)	259(7)	185(5)	148(4)	111(3)	111(3)
t4 min	15						
t5 max	74(2)						
t6	37(1)						
t7	185(5)	111(3)	111(3)	111(3)	111(3)	74(2)	74(2)

Notes

t0: delay between start of a read cycle and activation of WAIT

t1: delay between start of a read cycle and falling edge of CE and REG# (if required for the current cycle)

t2: delay between start of a read cycle and falling edge of OE# (and switching of the data buffer direction control)

t3: delay between falling edge of CE and falling edge of OE# (and switching of the data buffer direction control)

t4: read cycle length. This time is the necessary delay for the module to present the read data on the data output bus. After t4 delay is expired, WAIT is deasserted and ACK asserted thus enabling the processor to read the data on the bus. At the same time, ADLE is reset to latch the address presented to the module so that the data is not changed while the processor is reading. t4 can be lengthened by the module if the module requires extra wait cycles by asserting its WAIT# pin low.

t5: delay to deassertion of module read signal (OE# or IORD#) after minimum delay after t4.

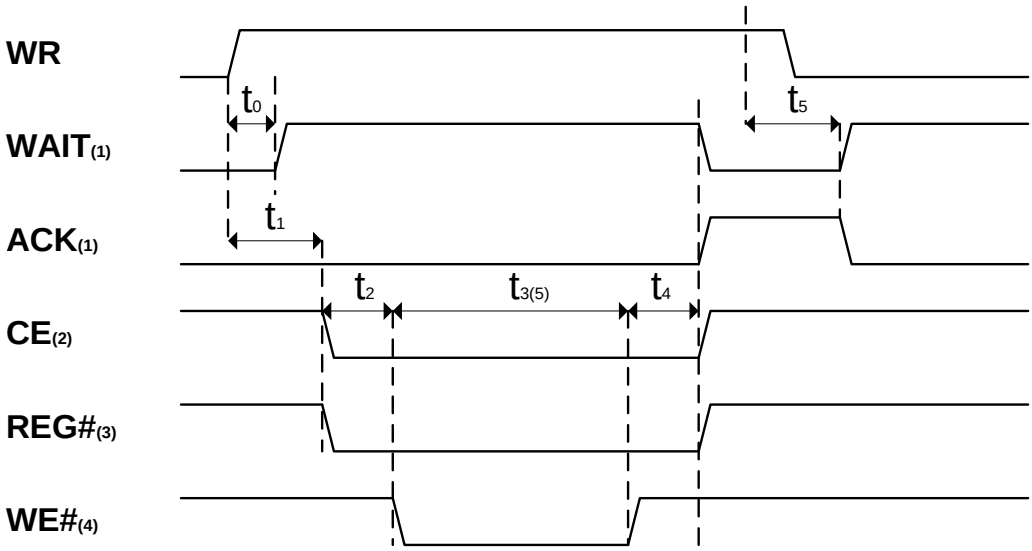
t6: delay between end of read cycle indicated by the processor and data bus isolation (DATOE# asserted)

t7: delay between data bus isolation and switching back of the data bus direction

t8: delay to deassertion of module read signal (OE# or IORD#) after end of a read cycle by the processor.

t7: delay between deassertion of the module read signal and re-enabling of the data bus (see t7 on write cycle)

5.4 Write Access



Notes

(1) The WAIT/ACK output is either WAIT or ACK formatted according to the WAIT/ACK pin settings (driving structure, active level)

(2) Depending on the write access type, CE can be either CE1A# or CE1B# for access to memory or IO mode to module A or B, CE2A# or CE2B# for access in EC(Extended Channel) mode, or even EXTCS for access to external device in regenerate mode.

(3) REG# signal is not asserted during a common memory or external access.

(4) WE# signal is asserted during a memory access(attribute or common). It is replaced by IOWR# during an IO write cycle, an EC write cycle, or an external device in regenerate mode.

(5) t3 can be lengthened by the insertion of wait cycles. When the module asserts WAIT# signal, t2 cycles counter stops until WAIT# becomes inactive anew.

Memory write timings are valid for both attribute and common memory mode. IO and external device in regenerate mode share the same timing specifications as they all use IORD# and IOWR# signals. Timings are given in CICORE1.0 clock cycles. They are calculated to comply with PCMCIA specifications when 27 MHz clock is used.

*unit: ns (cycle)

	Memory write					IO, EC, EXT
	600	250	200	150	100	
t0 max	15					
t1 max	74(2)					
t2	74(2)	37(2)				74(2)
t3	333(9)	185(5)	148(4)	111(3)	74(2)	185(5)
t4	74(2)	37(1)				37(1)
t5 max	15					

Notes

t0: delay between start of a write cycle and activation of WAIT

t1: delay between start of a write cycle and assertion of CE and REG# (if necessary for the current cycle)

t2: delay to assertion of the write signal (WE# or IOWR#) after the assertion of CE

t3: write cycle duration. This delay can be lengthened by the assertion of the module WAIT# pin

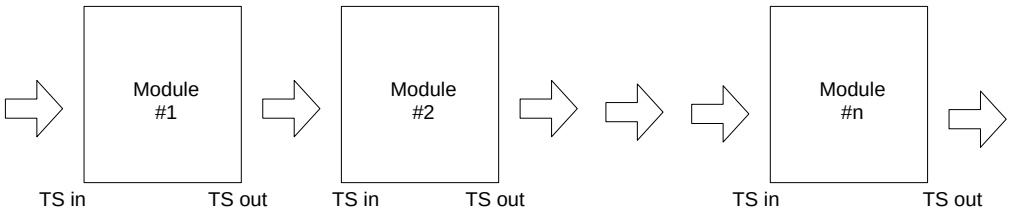
t4: delay between deassertion of the write signal and deassertion of CE, REG# and WAIT and assertion of ACK indicating to the processor the end of its write cycle

t5: delay between end of the write cycle and deassertion of ACK

6. MPEG Transport Stream Transition

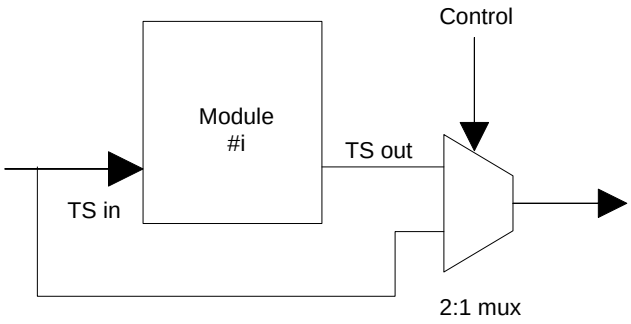
6.1 Transport Stream Daisy Chain

In the DVB Common Interface, each module has an MPEG input port constituted by MPEG clock, MPEG packet start, MPEG valid data and MPEG data bus and an MPEG output port composed of the same signals. The MPEG transport stream transits through the modules on a daisy chain basis.



6.2 Hot plug and Bypass Control

As a module can be inserted or removed at any time, the CICORE1.0 handles one MPEG transport stream bypass for each module. This bypass is enabled as long as a valid DVB CI module is not recognized to be inserted and activated in the corresponding slot or automatically as soon as the module is removed from a slot. The disabling of the bypass is controlled by the TSOEN bit in each Module Control Register.



6.3 Transport Stream / Addresses Input Signals

The MPEG input stream pins on the module are shared with the high order addresses specified by the PC card standard. When a module is inserted, before initialization, all these pins are forced to logical 0 state. If a memory module is recognized, the high order addresses A[25…15] can be applied to the module by setting the HAD bit in the Module Control Register. If a DVB module is recognized, the MPEG stream is applied to the module by setting the TSIEN bit in the Module Control Register. Those two bits cannot be set at the

same time and are reset when the module is extracted. The TSOEN bit (TS bypass control bit) can only be set when TSIEN has previously been set. Resetting TSIEN also resets TSOEN.

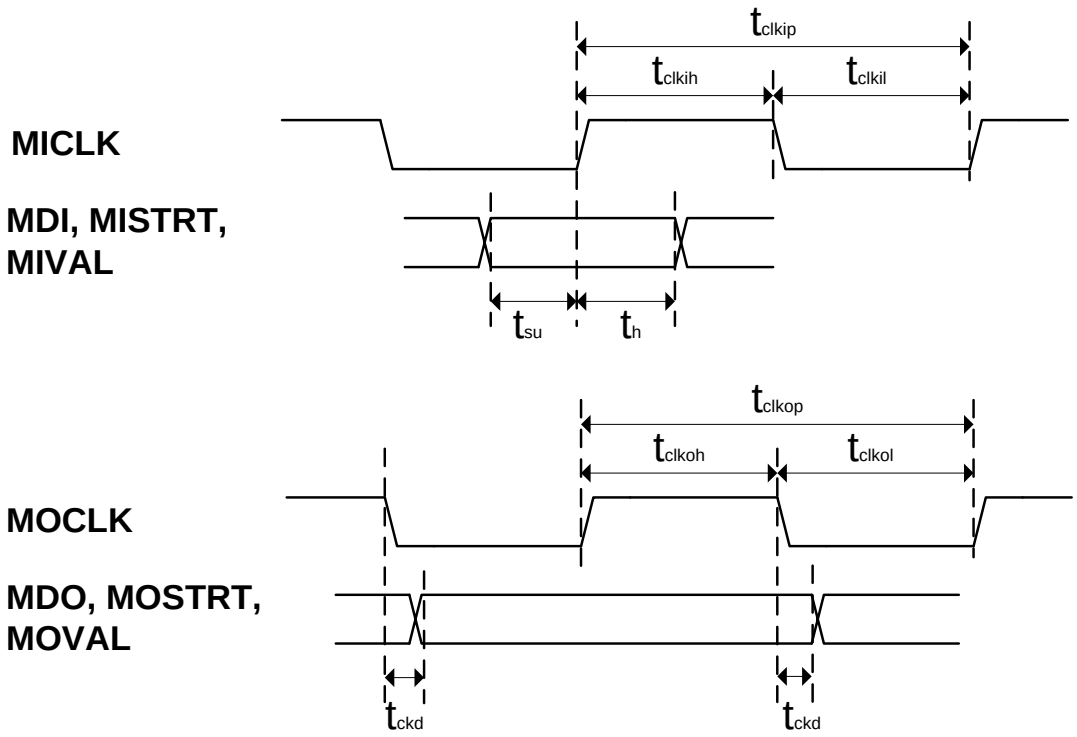
6.4 Invert Mask

Some modules can output an MPEG stream with inverted bits in the MPEG data bus. The CICORE1.0 is able to reinvert those bits to restore the correct data on the bus. This is achieved by setting the appropriate bits in the Invert Mask Register.

6.5 MPEG Signals

The MPEG inputs of the CICORE1.0 should be connected to the MPEG source of the host or from another CICORE1.0. MPEG signals coming from this source should respect the timing limits defined in the DVB standard. The MPEG outputs can be connected to any MPEG compliant destination or another CICORE1.0. MPEG output signals are guaranteed to meet the provided timing specifications.

6.6 Transport Stream Signal Timing



AC Electrical characteristics(VCC=5V, T=25°C)

Symbol	Item	MIN	MAX	Unit
t_{clkip}	MPEG input clock period	111		ns
t_{clkih}	MICLK input clock high time	40	97	ns
t_{clkil}	MICLK input clock low time	40	97	ns
t_{clkop}	MPEG output clock period	111		ns
t_{clkoh}	output clock high time	40	91	ns
t_{clkol}	output clock low time	40	91	ns
t_{su}	input data setup	15		ns
t_{h}	input data hold	10		ns
t_{ckd}	clock to data delay	0	15	ns

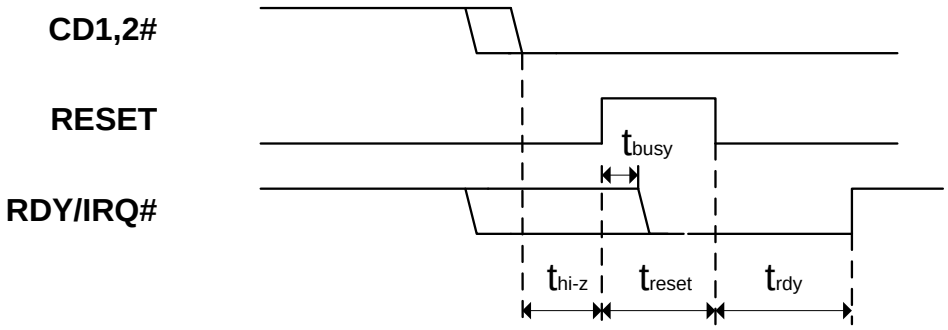
6.7 Command Interface Signals

The command interface is directly issued from PC Card standard restricted to 8 bits access and 15 bits addressing. The command interface of a CI module is described in detail in the PC Card standard and the restrictions applied to this standard for the command interface are described in the DVB CI standard.

The 15 address bits and 8 data bits of the CI modules are connected to the host microprocessor bus through tri-state buffers (type 373 and 245) which are controlled by the CICORE1.0 which outputs an output enable and a direction control signal for each buffer group.
CICORE1.0 provides the buffers control signals. The buffers should be powered by the same source as the modules.
The CI control signals are the same as the PC Card control signal : CE1, CE2, REG, OE, WE, IORD, IOWR, RDY/IRQ, WAIT. CICORE1.0 generates those signals so that they fit the PC Card standard whenever the host microprocessor accesses one of the modules.
The control signals activated depend on the access type chosen in the module control register with ACS[1:0]. The read and write signals active level duration is configured in the memory access cycle time registers. CICORE1.0 receives RDY/IRQ from the module and retransmits the interruption to the host microprocessor. The module can also send a WAIT request that is also transmitted to the host microprocessor in addition to the wait states already generated due to the read and write duration.

6.8 Module Detection and Activation

The CICORE1.0 automatically detects the insertion and removal of a module and acts as programmed whenever this occurs. In order to detect a module, two pins on the connector: CD1# and CD2# must be simultaneously asserted to ensure a module is inserted. When a module is inserted, the CICORE1.0 can automatically activate the module if programmed so when AUTO bit is asserted in the Module Control Register. The activation can also be handled manually by the host microprocessor by asserting the bits in the Module Control Register. The module activation consists in resetting the module and waiting for RDY signal to go high with respect to the PC card standard timings.



Symbol	Item	Min	Max	Unit
t_{hi-z}	Card detect to reset driven	300		ms
t_{reset}	Reset pulse width	11		µs
t_{busy}	Reset asserted to ready negated		10	µs
t_{rdy}	Reset negated to module ready		5	s

6.9 Interrupt

Interrupts are managed by CICORE1.0 and one interrupt output is available for connecting CICORE1.0 to the main microprocessor interrupt controller. Five interrupt sources are available: modules detection modules IRQ and one external device interrupt applied to the CICORE1.0 by using the external interrupt input pin. Modules detection interrupts are latched inside the CICORE1.0 and are acknowledged on the reading of the Interrupt Status Register. Each interrupt source can be individually masked. When masked, an incoming interrupt is visible in the Interrupt Status Register but does not generate an interrupt to the host microprocessor. The INT output to the host microprocessor can be configured to be active high or low and driven by a push-pull or an open drain.

6.10 Register Description

CICORE1.0 includes internal registers. All registers are reset to 00h. Register bits marked X should not be set. They are read as 0.

Register Address	Description
00	Module A Control Register
01	Module A auto select mask high Register
02	Module A auto select mask low Register
03	Module A auto select pattern high Register
04	Module A auto select pattern low Register
05	Memory access A cycle time Register
06	Invert Input Mask A Register
07	Reserved
08	Reserved
09	Module B Control Register
0A	Module B auto select mask high Register
0B	Module B auto select mask low Register
0C	Module B auto select pattern high Register
0D	Module B auto select pattern low Register
0E	Memory access B cycle time Register
0F	Invert Input Mask B Register
10	Reserved
11	Reserved
12	External access auto select mask high Register
13	External access auto select mask low Register
14	External access auto select pattern high Register
15	External access auto select pattern low Register
16	Reserved
17	Destination select Register
18	Power control Register
19	Reserved
1A	Interrupt Status Register
1B	Interrupt Mask Register
1C	Interrupt Config Register
1D	Microprocessor Interface Config Register
1E	Microprocessor wait/ack Config Register
1F	CICORE1.0 Control Register

6.11 Registers Information

Address	Description
'h00 ('h09)	Module A (Module B) control register

RST	TSOEN	TSIEN	HAD	ACS1	ACS0	AUTO	DET

- RST — RST pin control of common interface(CI) modules
  Only able to be set when DET=1
  Forced to 0 when DET=0

- TSOEN — MPEG transport stream bypass control
  Only able to be set when DET=1 and HAD=0 and TSIEN=1
  Forced to 0 when DET=0 or TSIEN=0
  0 : bypass enabled
  1 : bypass disabled

- TSIEN — MPEG transport stream input control
  Only able to be set when DET=1 and HAD=0
  Forced to 0 when DET=0
  0 : no MPEG stream
  1 : MPEG stream enabled

- HAD — High order addresses in place of MPEG stream input
  Only able to be set when DET=1 and TSIEN=0 and TSOEN=0
  Forced to 0 when DET=0
  0 : apply MPEG stream
  1 : apply A[25:15] for memory access

- ACS[1:0] — Module access type
  Only able to be set when DET=1
  Forced to "00" when DET=0
  00 : access to attribute memory
  01 : access to I/O space
  10 : access to common memory

- AUTO — Module auto activation on detection
  0 : no auto activation procedure

1 : start module auto activation when DET=1 and module power on

• DET Module detection

0 : no module present

1 : module inserted

'h01 Module A (Module B) auto select mask high register ('h0A)

X	X	X	X	X	MA25	MA24	MA23

'h02 Module A (Module B) auto select mask low register ('h0B)

MA22	MA21	MA20	MA19	MA18	MA17	MA16	MA15

• MA[25:15] Address mask for decoding

0 : address bit doesn't care

1 : address bit should match programmed address bit in module auto select pattern register

'h03 Module A (Module B, External) auto select pattern high register ('h0C,'h14)

X	X	X	X	X	PA25	PA24	PA23

'h04 Module A (Module B, External) auto select pattern low register ('h0D,'h15)

PA22	PA21	PA20	PA19	PA18	PA17	PA16	PA15

• PA[25:15] Address pattern to match in accordance with address mask to select the corresponding module.

Relevant only when DEF=0 in external auto select mask. Doesn't care if DEF=1.

'h05 Module A (Module B) Memory access cycle time register ('h0E)

X	AM2	AM1	AM0	X	CM2	CM1	CM0

• AM[2:0] Attribute memory cycle time used

000 : 100ns

001 : 150ns

010 : 200ns

011 : 250ns

100 : 600ns

101 to 111: reserved.

Do not use.

This timing is valid for write access. During read access, if AM=100, 600ns cycles will be used,

if AM=0XX, 300ns will be used.

- CM[2:0] Common memory cycle time used

000 : 100ns

001 : 150ns

010 : 200ns

011 : 250ns

100 : 600ns

101 to 111 : reserved. Do not use

'h06 ('h0F) Module A (Module B) Invert input mask register

INV7	INV6	INV5	INV4	INV3	INV2	INV1	INV0

- INV[7:0] Invert mask

0 : corresponding bit is not complemented

1 : corresponding bit is complemented

'h12 External access auto select mask high register

DEF	X	X	X	X	MA25	MA24	MA23

'h13 External access auto select mask low register

MA22	MA21	MA20	MA19	MA18	MA17	MA16	MA15

- DEF External device default addressing

0 EXTCS asserted when address match mask and pattern

1 EXTCS asserted when neither module A nor module B is selected while CS input active

• MA[25:15] Address mask for decoding

Relevant only when DEF=0. Doesn't care if DEF=1.

0 : address bit doesn't care

1 : address bit should match programmed address bit in module auto select pattern register

* 'h17 Destination select register

X	X	XCSDRV	XCSLVL	XCSMOD	SEL1	SEL0	AUTOSEL

• XCSDRV EXTCS output pin structure

Changing this bit is only allowed when LOCK=0

0 : EXTCS buffer is open-drain

1 : EXTCS buffer is push-pull

• XCSLVL EXTCS output pin active level

Changing this bit is only allowed when LOCK=0

0 : EXTCS pin is active-low

1 : EXTCS pin is active-high

• XCSMOD EXTCS generation mode

Changing this bit is only allowed when LOCK=0

0 : transmit EXTCS

1 : Regenerate EXTCS (default)

• SEL[1:0] Module select

Relevant only when AUTOSEL=0

00 : no destination selected

01 : select module A

10 : select module B

11 : select external device using EXTCS

• AUTOSEL Automatic module selection

Uses high order addresses to choose module or external device (using EXTCS)

0 : manual selection

1 : automatic selection

'h18 Power control register

VCDRV	VCLVL	X	VAUTO	VCCEB	VCCEA	X	VCC

• VCDRV Module VCC output pin structure

Changing this bit is only allowed when LOCK=0

0 : VCC buffer is open-drain

1 : VCC buffer is push-pull

• VCLVL Module VCC output pin active level

Changing this bit is only allowed when LOCK=0

0 : VCC pin is active-low

1 : VCC pin is active-high

• VAUTO Automatic module power on by module detection

Changing this bit is only allowed when LOCK=1

0 : disable autom power-on

1 : enable auto power-on

• VCCEB Module power supply switch control for Module B

Changing this bit is only allowed when LOCK=1

0 : power off

1 : power on

• VCCEA Module power supply switch control for Module A

Module power supply switch control for both Module A and B

0 : power off

1 : power on

• VCC Module power supply switch control

Changing this bit is only allowed when LOCK=1

0 : power off

1 : power on

'h1A Interrupt status register

X	X	X	EXT	IRQB	IRQA	DETB	DETA

• EXT EXTINT status

0 : EXTINT is inactive

1 : EXTINT is active

- IRQB Slot B inverted IRQ line state

  0 : IRQ on slot B is high(inactive)

  1 : IRQ on slot B is low(active)

- IRQA Slot A inverted IRQ line state

  0 : IRQ on slot A is high(inactive)

  1 : IRQ on slot A is low(active)

- DETB Slot B module detection

  Reset on read

  0 : no change

  1 : a module has been inserted or extracted in slot B

- DETA Slot A module detection

  Reset on read

  0 : no change

  1 : a module has been inserted or extracted in slot A

'h1B Interrupt mask register

0	0	0	EXTM	IRQBM	IRQAM	DETBM	DETAM

- EXTM External interrupt mask

  0 : masked

  1 : unmasked : an interrupt request from external source will be transmitted to the microprocessor

- IRQBM Slot B IRQ mask

  0 : masked

  1 : unmasked : an interrupt request from module B will be transmitted to the microprocessor

- IRQAM Slot A IRQ mask

  0 : masked

  1 : unmasked : an interrupt request from module A will be transmitted to the microprocessor

- DETBM Slot B module detection mask

  Reset on read

  0 : masked

1 : unmasked : a module movement in slot B will generate an interrupt

• DETAM Slot A module detection mask

0 : masked

1 : unmasked : a module movement in slot A will generate an interrupt

'h1C Interrupt configure register

X	X	X	X	X	ITDRV	ITLVL	EXTLVL

• ITDRV INT output pin structure

Changing this bit is only allowed when LOCK=0

0 : INT buffer is open-drain

1 : INT buffer is push-pull

• ITLVL INT output pin active level

Changing this bit is only allowed when LOCK=0

0 : INT pin is active-low

1 : INT pin is active-high

• EXTLVL EXTINT input pin active level

Changing this bit is only allowed when LOCK=0

0 : EXTINT pin is active-low

1 : EXTINT pin is active-high

'h1D Microprocessor interface config register

ALLVL	DDLVL	X	X	CSLVL	WSTRLVL	RDIRLVL	RDIR

• ALLVL ADLE active level

Changing this bit is only allowed when LOCK=0

0 : ADLE is active-high (default)

1 : ADLE is active-low

• DDLVL DATDIR active level

Changing this bit is only allowed when LOCK=0

0 : high for read (default)

1 : low for read

• CSLVL CS input active level

Changing this bit is only allowed when LOCK=0

0 : CS is active-low

1 : CS is active-high

• WSTRLVL WR/STR input active level

Changing this bit is only allowed when LOCK=0

0 : WR/STR is active-low

1 : WR/STR is active-high

• RDIRLVL RD/DIR input active level

Changing this bit is only allowed when LOCK=0

0 : RD is active-low or RD/DIR input is low during read transfer and high during write

1 : RD is active-high or RD/DIR input is high during read transfer and high during write

• RDIR RD/DIR and WR/STR inputs function

Changing this bit is only allowed when LOCK=0

0 : RD/WR mode

1 : DIR/STR mode

'h1E Microprocessor wait/ack config register

X	X	X	X	X	WACK	WDRV	WLVL

• WACK WAIT/ACK pin function

Changing this bit is only allowed when LOCK=0

0 : WAIT mode

1 : ACK mode

• WDRV WAIT/ACK output pin structure

Changing this bit is only allowed when LOCK=0

0 : WAIT/ACK buffer is open-drain

1 : WAIT/ACK buffer is push-pull

• WLVL WAIT/ACK output pin active level

Changing this bit is only allowed when LOCK=0

0 : WAIT/ACK pin is active-low

1 WAIT/ACK pin is active-high

'h1F CIPRO control register

RST	X	X	X	0	0	EIAA	LOCK

- RST Reset chip

  1 : reset

- EIAA Early Interrupt for Auto Activation

  0 : Interrupt at the end of auto activation

  1 : Interrupt at the start of auto activation

- LOCK Validates and locks the chip setup

  0 : chip is not configured.

  1 : chip is configured

7. Electrical Characteristics

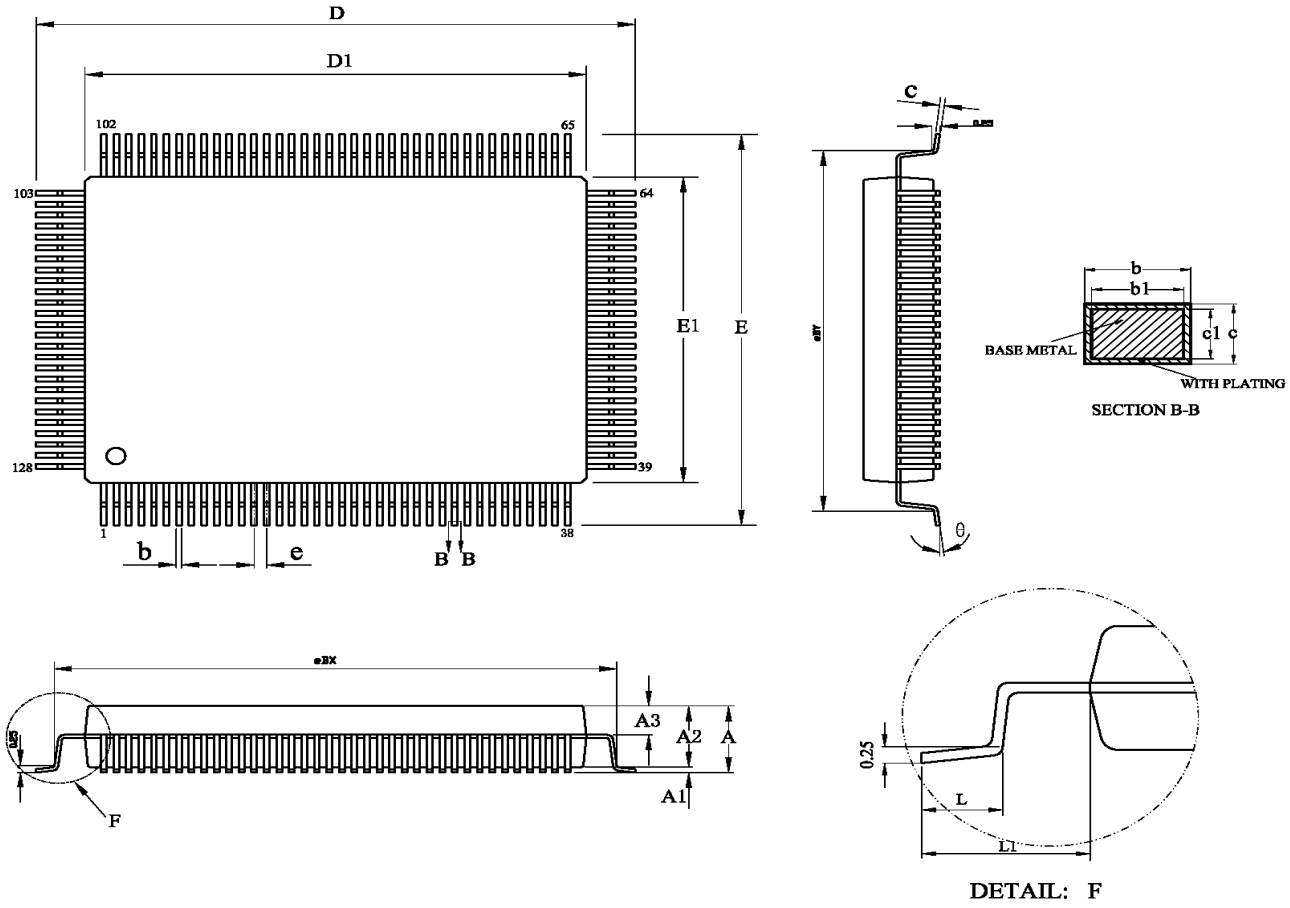
DC Characteristics

Symbol	Parameter	Minimum		Maximum		Conditions	
		TTL	CMOS	TTL	CMOS	V_{DD}	
V_{IL}	Input Low Level Voltage	-0.5V	-0.5V	0.8V	$0.3xV_{DD}$	2.7V to 3.6V	Guaranteed Input Low Voltage
V_{IH}	Input High Level Voltage	2.0V	$0.7xV_{DD}$	V_{DD} + 0.5V	V_{DD}+ 0.5V	2.7V to 3.6V	Guaranteed Input High Voltage
V_{OL}	Output Low Level Voltage			0.4V	V_{SS}+0.1V	2.7V	I_{OL} = 0.8mA(CMOS) = 2 to 0.8mA(TTL)
V_{OH}	Output High Level Voltage	2.4V	V_{DD}-0.1V			2.7V	I_{OH}=0.8mA(CMOS) = 2 to 0.8mA(TTL)
I	Input Current at maximum voltage			1mA	1mA	2.7V to 3.6V	Input = 5.5V

Recommended Operating Conditions

Symbol	Parameter	Min	Max	Condition
	Power Supply	2.7V	3.6V	
V_{IL}	Input Low Level Voltage			Guaranteed Input Low Voltage
	CMOS input	-0.33V	$0.2xV_{DD}$	
	TTL input	-0.33V	0.8V	
V_{IH}	Input High Level Voltage			Guaranteed Input High Voltage
	CMOS input	$0.7xV_{DD}$	$V_{DD}+0.5V$	
	TTL input	2.0V	$V_{DD}+0.5V$	
	Junction Temperature	0℃	100℃	

8. Package Dimension



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	3.20
A1	0.15	—	0.35
A2	2.70	2.75	2.80
A3	1.25	1.30	1.35
b	0.18	—	0.28
b1	0.17	0.20	0.23
c	0.15	—	0.20
c1	0.14	0.15	0.16
D	23.00	23.20	23.40
D1	19.90	20.00	20.10
E	17.00	17.20	17.40
E1	13.90	14.00	14.10
eBX	21.75	—	21.95
eBY	15.75	—	15.95
e	0.50BSC		
L	0.73	—	1.03
L1	1.60BSC		
θ	0	—	7°