



CI Core2.0

Dual Common Interface Hardware Controller
for Multiple Tuner Digital Satellite Video Receiver

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Table of Contents

| | |
|--|----|
| 1. PRODUCT OVERVIEW | 4 |
| 2. FEATURES..... | 5 |
| 3. BLOCK DIAGRAM..... | 6 |
| 4. PIN CONFIGURATION | 7 |
| 5. PIN DESCRIPTION | 8 |
| 6. HOST MICROPROCESSOR INTERFACE..... | 13 |
| 6.1 CONFIGURATION INTERFACE | 13 |
| 6.2 UNIVERSAL MICROPROCESSOR CONTROL SIGNAL GENERATOR (UCSG) | 14 |
| 6.3 READ ACCESS..... | 15 |
| 6.4 WRITE ACCESS | 17 |
| 6.4 MPEG TRANSPORT STREAM CONTROL | 18 |
| 7. MPEG TRANSPORT STREAM TRANSITION | 20 |
| 7.1 TS DAISY CHAIN..... | 20 |
| 7.2 HOT PLUG AND BYPASS CONTROL | 20 |
| 7.3 TS/ADDRESSES INPUT SIGNALS | 20 |
| 7.4 INVERT MASK | 22 |
| 7.5 MPEG SIGNALS | 22 |
| 7.6 TS SIGNALS TIMING..... | 22 |
| 7.7 COMMAND INTERFACE SIGNALS | 23 |
| 7.8 MODULE DETECTION AND ACTIVATION | 24 |
| 7.9 INTERRUPTS | 24 |
| 7.10 REGISTERS DESCRIPTION..... | 25 |
| 7.11 REGISTERS INFORMATION | 27 |
| 8. ELECTRICAL CHARACTERISTICS | 39 |
| 9. PACKAGE DIMENSION | 41 |

1. Product Overview

CICORE2.0 is the common interface controller for digital satellite video receiver and digital TV to adopt the common interface standard (CENELEC EN-50221).

Through CICORE2.0, a microprocessor of receiver reads the status of the common interface modules and gives a command to the modules, which process the MPEG video stream.

After CICORE2.0 is initialized by I2C bus connected with the microprocessor, it generates the command interface control signals to meet the specification of each module from the control signals of the microprocessor. CICORE2.0 supports the interface of various kinds of microprocessors for flexible implementation of the receiver. CICORE2.0 is able to control two independent modules simultaneously and to support hot-insertion of them.

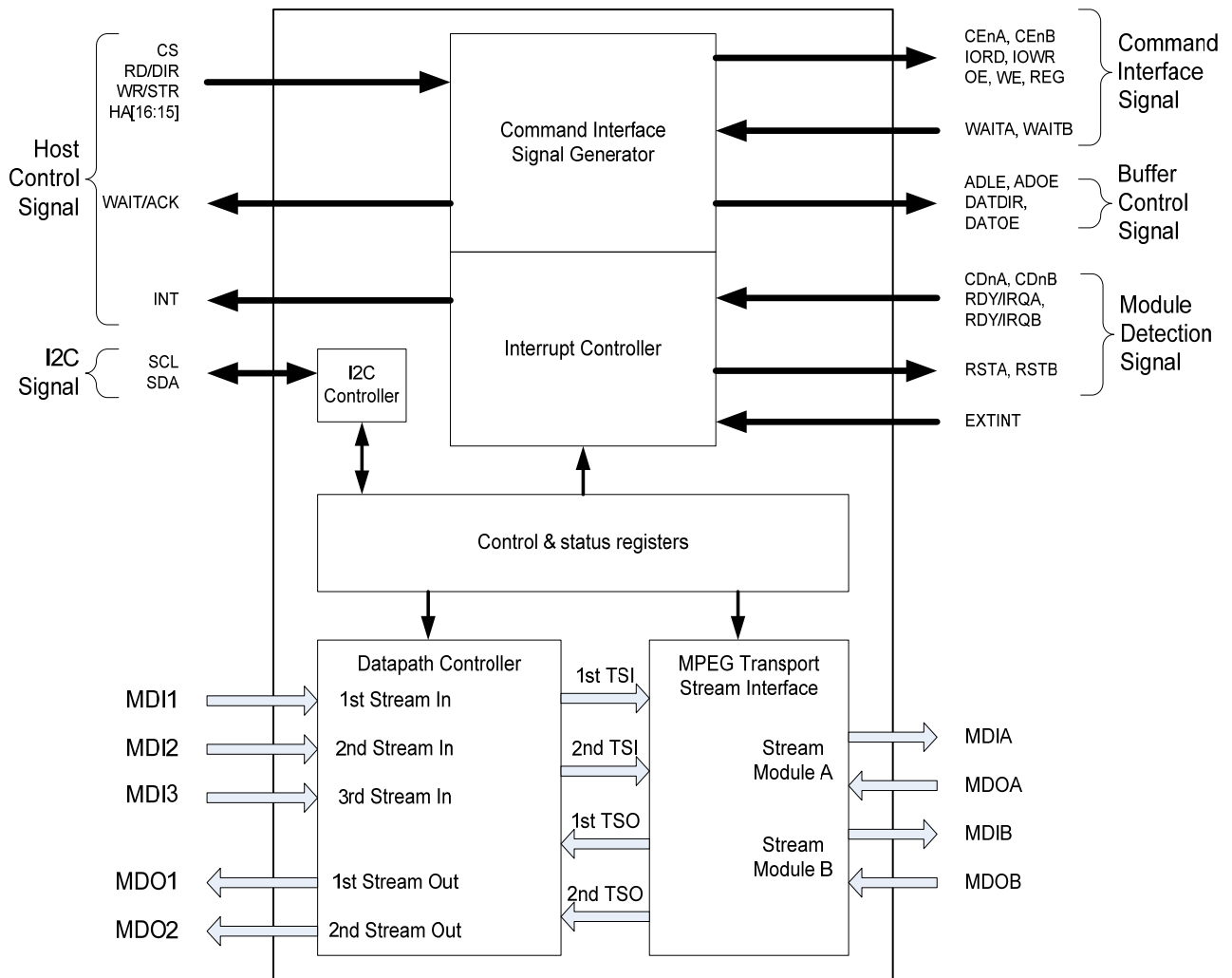
CICORE2.0 receives two independent MPEG Transport streams primarily. If necessary, CICORE2.0 can receive another MPEG Transport stream. By processing one or two of the MPEG Transport streams selectively, CICORE2.0 is also able to output two independent MPEG video streams.

In addition, instead of the common interface modules, CICORE2.0 supports an 8-bit memory card based on PC Card Standard, which enables a receiver to extend its memory size.

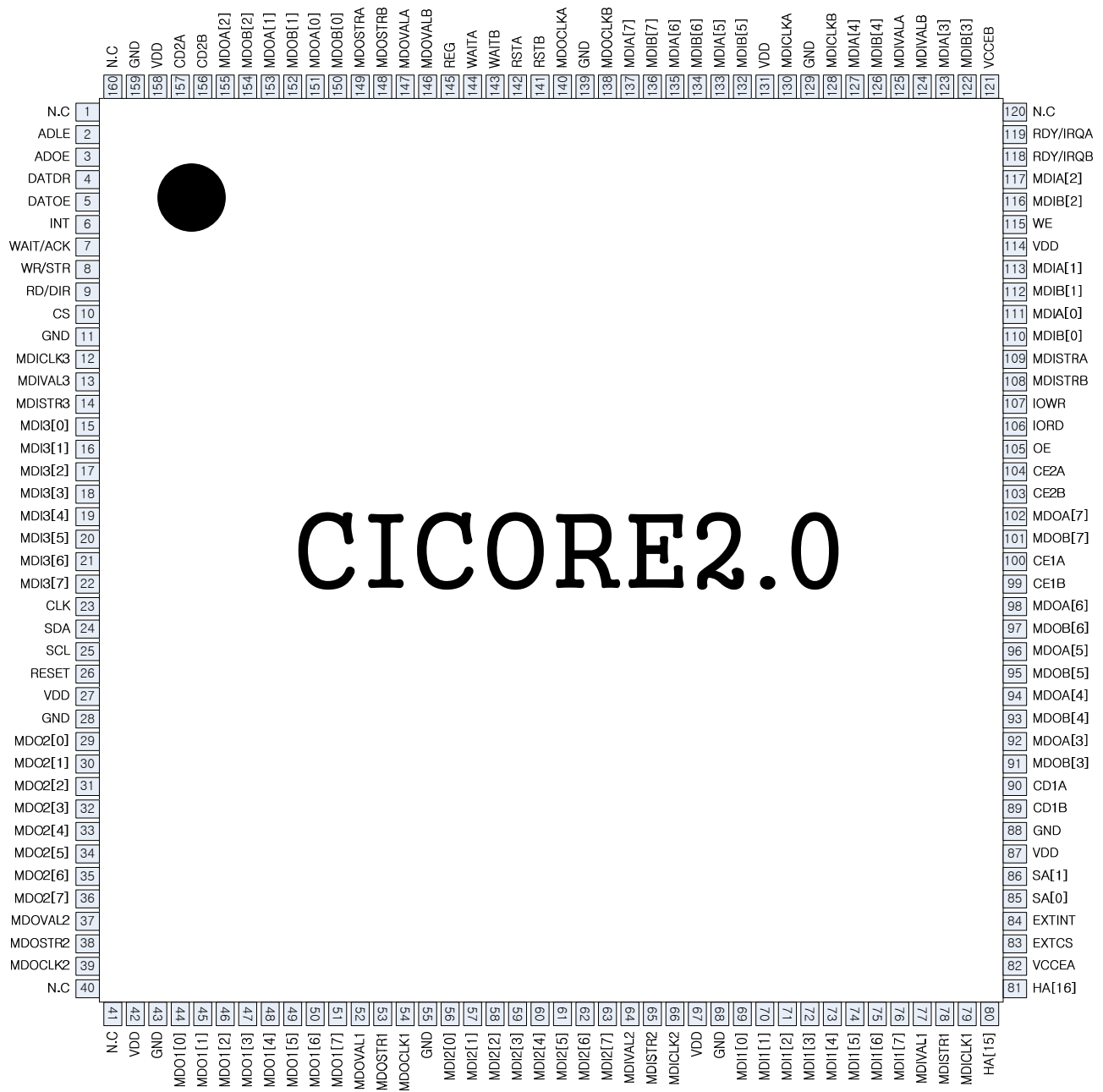
2. Features

- Module Interface
 - 2 full independent module capability
 - Common Interface Standard compliant
- DVB_CI (CENELEC EN-50221)
- NRSS-B (SCTE IS-679 Part B)
- DAVIC v1.2 (CA0 interface)
- Memory PCMCIA compliance (R2)
- 8-bit data access
- 26-bit address Memory Card
- Attribute Memory access (CIS, Tuple)
- High speed capability
- Up to 20Mbits/s on Command Interface
- Up to 100Mbits/s on Transport Stream
- Polling and Interrupt modes
- Hot Insertion (Automatic and Reset VCC handling)
- 5V tolerant I/O for common interface
- LQFP 160 package
- Host microprocessor Interface
 - Universal Control Signal Generator (UCSG)
 - PC Card control signals generation
 - Supports PowerPC, ARM, ST20, 68xxx, TMS, LSI 64008, TC81220F, IDTR3041 host microprocessors
 - I²C port
- CICORE2.0 Set-up
- Slot selection
 - Cascade mode management
 - Chip Select bank and Interrupt facilities
 - 3.3V for all I/O buffers
- Digital Video Stream Interface
 - MPEG II Transport Stream compliant
 - Simultaneous processing two MPEG streams
- Maximum 3 TS(Transport Stream) inputs and 2 TS outputs
- 3.3V I/O buffer for direct interface with FEC and DEMUX ICs

3. Block Diagram



4. Pin Configuration



5. Pin Description

| Pin Number | Name | I/O | Type | Description |
|------------|----------|-----|-----------|--|
| 1 | N.C | | | |
| 2 | ADLE | O | CMOS | External address buffer latch enable signal |
| 3 | ADOE | O | CMOS | External address buffer output enable signal |
| 4 | DATDR | O | CMOS | External data buffer direction |
| 5 | DATOE | O | CMOS | External data buffer output enable |
| 6 | INT | O | CMOS TS | Interrupt output to microprocessor |
| 7 | WAIT/ACK | O | CMOS TS | Wait or acknowledge signal to microprocessor |
| 8 | WR/STR | I | CMOS | Write or strobe signal from microprocessor |
| 9 | RD/DIR | I | CMOS | Read or direction signal from microprocessor |
| 10 | CS | I | CMOS | Chip select signal from microprocessor |
| 11 | GND | | Power | |
| 12 | MDICLK3 | I | CMOS | MPEG clock signal input 3 |
| 13 | MDIVAL3 | I | CMOS | MPEG data valid signal input 3 |
| 14 | MDISTR3 | I | CMOS | MPEG data start signal input 3 |
| 15 | MDI3[0] | I | CMOS | MPEG data input 3 |
| 16 | MDI3[1] | I | CMOS | MPEG data input 3 |
| 17 | MDI3[2] | I | CMOS | MPEG data input 3 |
| 18 | MDI3[3] | I | CMOS | MPEG data input 3 |
| 19 | MDI3[4] | I | CMOS | MPEG data input 3 |
| 20 | MDI3[5] | I | CMOS | MPEG data input 3 |
| 21 | MDI3[6] | I | CMOS | MPEG data input 3 |
| 22 | MDI3[7] | I | CMOS | MPEG data input 3 |
| 23 | CLK | I | CMOS | Clock Input – 27 MHz |
| 24 | SDA | I/O | CMOS trig | I2C data |
| 25 | SCL | I | CMOS trig | I2C clock |
| 26 | RESET | I | CMOS | Chip reset – high active |
| 27 | VDD | | Power | |
| 28 | GND | | Power | |
| 29 | MDO2[0] | O | CMOS | MPEG data output 2 |
| 30 | MDO2[1] | O | CMOS | MPEG data output 2 |

| | | | | |
|----|---------|---|-------|---------------------------------|
| 31 | MDO2[2] | O | CMOS | MPEG data output 2 |
| 32 | MDO2[3] | O | CMOS | MPEG data output 2 |
| 33 | MDO2[4] | O | CMOS | MPEG data output 2 |
| 34 | MDO2[5] | O | CMOS | MPEG data output 2 |
| 35 | MDO2[6] | O | CMOS | MPEG data output 2 |
| 36 | MDO2[7] | O | CMOS | MPEG data output 2 |
| 37 | MDOVAL2 | O | CMOS | MPEG data valid signal output 2 |
| 38 | MDOSTR2 | O | CMOS | MPEG data start signal output 2 |
| 39 | MDOCLK2 | O | CMOS | MPEG data clock signal output 2 |
| 40 | N.C. | | | |
| 41 | N.C. | | | |
| 42 | VDD | | Power | |
| 43 | GND | | Power | |
| 44 | MDO1[0] | O | CMOS | MPEG data output 1 |
| 45 | MDO1[1] | O | CMOS | MPEG data output 1 |
| 46 | MDO1[2] | O | CMOS | MPEG data output 1 |
| 47 | MDO1[3] | O | CMOS | MPEG data output 1 |
| 48 | MDO1[4] | O | CMOS | MPEG data output 1 |
| 49 | MDO1[5] | O | CMOS | MPEG data output 1 |
| 50 | MDO1[6] | O | CMOS | MPEG data output 1 |
| 51 | MDO1[7] | O | CMOS | MPEG data output 1 |
| 52 | MDOVAL1 | O | CMOS | MPEG data valid signal output 1 |
| 53 | MDOSTR1 | O | CMOS | MPEG data start signal output 1 |
| 54 | MDOCLK1 | O | CMOS | MPEG data clock signal output 1 |
| 55 | GND | | Power | |
| 56 | MDI2[0] | I | CMOS | MPEG data input 2 |
| 57 | MDI2[1] | I | CMOS | MPEG data input 2 |
| 58 | MDI2[2] | I | CMOS | MPEG data input 2 |
| 59 | MDI2[3] | I | CMOS | MPEG data input 2 |
| 60 | MDI2[4] | I | CMOS | MPEG data input 2 |
| 61 | MDI2[5] | I | CMOS | MPEG data input 2 |
| 62 | MDI2[6] | I | CMOS | MPEG data input 2 |
| 63 | MDI2[7] | I | CMOS | MPEG data input 2 |
| 64 | MDIVAL2 | I | CMOS | MPEG data valid signal input 2 |
| 65 | MDISTR2 | I | CMOS | MPEG data start signal input 2 |

| | | | | |
|----|---------|---|-----------------|--|
| 66 | MDICK2 | I | CMOS | MPEG clock signal input 2 |
| 67 | VDD | | Power | |
| 68 | GND | | Power | |
| 69 | MDI1[0] | I | CMOS | MPEG data input 1 |
| 70 | MDI1[1] | I | CMOS | MPEG data input 1 |
| 71 | MDI1[2] | I | CMOS | MPEG data input 1 |
| 72 | MDI1[3] | I | CMOS | MPEG data input 1 |
| 73 | MDI1[4] | I | CMOS | MPEG data input 1 |
| 74 | MDI1[5] | I | CMOS | MPEG data input 1 |
| 75 | MDI1[6] | I | CMOS | MPEG data input 1 |
| 76 | MDI1[7] | I | CMOS | MPEG data input 1 |
| 77 | MDIVAL1 | I | CMOS | MPEG data valid signal input 1 |
| 78 | MDISTR1 | I | CMOS | MPEG data start signal input 1 |
| 79 | MDICK1 | I | CMOS | MPEG clock signal input 1 |
| 80 | HA[15] | I | CMOS up | Optional mode Address bit 15 of microprocessor |
| 81 | HA[16] | I | CMOS up | Optional mode Address bit 16 of microprocessor |
| 82 | VCCEA | O | CMOS TS | VCC switch control signal of modules |
| 83 | EXTCS | O | CMOS TS | Chip select signal of external device |
| 84 | EXTINT | I | CMOS | Interrupt signal of external device |
| 85 | SA[0] | I | CMOS | I2C address bit 0 |
| 86 | SA[1] | I | CMOS | I2C address bit 1 |
| 87 | VDD | | Power | |
| 88 | GND | | Power | |
| 89 | CD1B | I | CMOS trig up | Card detect signal 1 of module B |
| 90 | CD1A | I | CMOS trig up | Card detect signal 1 of module A |
| 91 | MDOB[3] | I | CMOS up | MPEG data input from module B |
| 92 | MDOA[3] | I | CMOS up | MPEG data input from module A |
| 93 | MDOB[4] | I | CMOS up | MPEG data input from module B |
| 94 | MDOA[4] | I | CMOS up | MPEG data input from module A |
| 95 | MDOB[5] | I | CMOS up | MPEG data input from module B |
| 96 | MDOA[5] | I | CMOS up | MPEG data input from module A |
| 97 | MDOB[6] | I | CMOS up | MPEG data input from module B |
| 98 | MDOA[6] | I | CMOS up | MPEG data input from module A |

| | | | | |
|-----|----------|---|---------|--------------------------------------|
| 99 | CE1B | O | CMOS TS | Card enable signal 1 of module B |
| 100 | CE1A | O | CMOS TS | Card enable signal 1 of module A |
| 101 | MDOB[7] | I | CMOS up | MPEG data input from module B |
| 102 | MDOA[7] | I | CMOS up | MPEG data input from module A |
| 103 | CE2B | O | CMOS TS | Card enable signal 2 of module B |
| 104 | CE2A | O | CMOS TS | Card enable signal 2 of module A |
| 105 | OE | O | CMOS TS | Output enable signal to modules |
| 106 | IORD | O | CMOS TS | I/O read signal to modules |
| 107 | IOWR | O | CMOS TS | I/O write signal to modules |
| 108 | MDISTRB | O | CMOS TS | MPEG data start signal to module B |
| 109 | MDISTRA | O | CMOS TS | MPEG data start signal to module A |
| 110 | MDIB[0] | O | CMOS TS | MPEG data output to module B |
| 111 | MDIA[0] | O | CMOS TS | MPEG data output to module A |
| 112 | MDIB[1] | O | CMOS TS | MPEG data output to module B |
| 113 | MDIA[1] | O | CMOS TS | MPEG data output to module A |
| 114 | VDD | | Power | |
| 115 | WE | O | CMOS TS | Write enable signal to modules |
| 116 | MDIB[2] | O | CMOS TS | MPEG data output to module B |
| 117 | MDIA[2] | O | CMOS TS | MPEG data output to module A |
| 118 | RDY/IROB | I | CMOS | RDY/IRQ signal from module B |
| 119 | RDY/IROA | I | CMOS | RDY/IRQ signal from module A |
| 120 | N.C. | | | |
| 121 | VCCEB | | | VCC switch control signal of modules |
| 122 | MDIB[3] | O | CMOS TS | MPEG data output to module B |
| 123 | MDIA[3] | O | CMOS TS | MPEG data output to module A |
| 124 | MDIVALB | O | CMOS TS | MPEG data valid signal to module B |
| 125 | MDIVALA | O | CMOS TS | MPEG data valid signal to module A |
| 126 | MDIB[4] | O | CMOS TS | MPEG data output to module B |
| 127 | MDIA[4] | O | CMOS TS | MPEG data output to module A |
| 128 | MDICLKB | O | CMOS TS | MPEG clock signal output to module B |
| 129 | GND | | Power | |
| 130 | MDICLKA | O | CMOS TS | MPEG clock signal output to module A |
| 131 | VDD | | Power | |
| 132 | MDIB[5] | O | CMOS TS | MPEG data output to module B |
| 133 | MDIA[5] | O | CMOS TS | MPEG data output to module A |

| | | | | |
|-----|---------|---|-----------------|---------------------------------------|
| 134 | MDIB[6] | O | CMOS TS | MPEG data output to module B |
| 135 | MDIA[6] | O | CMOS TS | MPEG data output to module A |
| 136 | MDIB[7] | O | CMOS TS | MPEG data output to module B |
| 137 | MDIA[7] | O | CMOS TS | MPEG data output to module A |
| 138 | MDOCLKB | I | CMOS up | MPEG clock signal input from module B |
| 139 | GND | | Power | |
| 140 | MDOCLKA | I | CMOS up | MPEG clock signal input from module A |
| 141 | RSTB | O | CMOS TS | Reset of module B |
| 142 | RSTA | O | CMOS TS | Reset of module A |
| 143 | WAITB | I | CMOS | WAIT signal of module B |
| 144 | WAITA | I | CMOS | WAIT signal of module A |
| 145 | REG | O | CMOS TS | REG signal to modules |
| 146 | MDOVALB | I | CMOS up | MPEG data valid input from module B |
| 147 | MDOVALA | I | CMOS up | MPEG data valid input from module A |
| 148 | MDOSTRB | I | CMOS up | MPEG data start input from module B |
| 149 | MDOSTRA | I | CMOS up | MPEG data start input from module A |
| 150 | MDOB[0] | I | CMOS up | MPEG data input from module B |
| 151 | MDOA[0] | I | CMOS up | MPEG data input from module A |
| 152 | MDOB[1] | I | CMOS up | MPEG data input from module B |
| 153 | MDOA[1] | I | CMOS up | MPEG data input from module A |
| 154 | MDOB[2] | I | CMOS up | MPEG data input from module B |
| 155 | MDOA[2] | I | CMOS up | MPEG data input from module A |
| 156 | CD2B | I | CMOS trig up | Card detect signal 2 of module B |
| 157 | CD2A | I | CMOS trig up | Card detect signal 2 of module A |
| 158 | VDD | | Power | |
| 159 | GND | | Power | |
| 160 | N.C | | | |

Note : TTL(TTL level), CMOS(CMOS level), TS(Tristate),
up(internal pull-up), down(internal pull-down), trig(Schmitt trigger)

6. Host Microprocessor Interface

6.1 Configuration interface

CICORE2.0 needs a clock source of 27MHz frequency with its duty cycle of 33% to 67%. This clock source is commonly available in any digital video system.

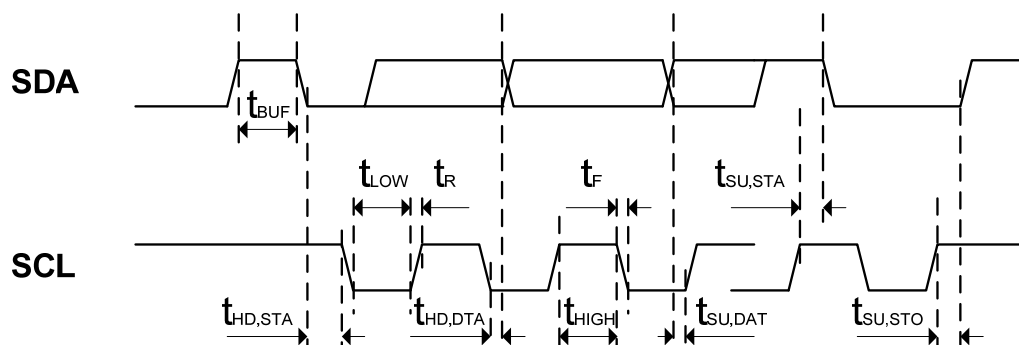
CICORE2.0 is configured by accessing the various registers through a standard I²C interface. The I²C device address is chosen among four values by connecting SA1 and SA0 to VCC or GND.

The base address can be chosen among 80h, 82h, 84h, and 86h. So maximum 4 CICORE2.0 devices can be connected to one microprocessor. Refer to I²C standard of Philips data book for the detailed AC/DC characteristics and the timing diagram of the I²C interface.

CICORE2.0 can control various kinds of microprocessors. By reset, the host microprocessor interface is disabled – CS, RD/DIR and WR/STR inputs are in inactive state and WAIT/ACK and INT are in high impedance state. Only the Interface for CICORE2.0 configuration is available. Once CICORE2.0 is configured, the other interface is enabled by setting the LOCK bit in the control register('h1F). Then its modules are accessible and some parameters for host microprocessor interface are disabled from modification.

Host microprocessor input control signals are CS, RD/DIR, WR/STR. Output signals are WAIT/ACK and INT. Active levels of input and output can be individually set up by configuration bits. The output buffer structure is also configurable to be either open-drain or push-pull. CICORE2.0 inputs the RD/DIR, WR/STR, and CS signals from host microprocessor, WAITA, and WAITB from the modules. It generates all the control signals to modules, host microprocessor, buffers and external device: CE1A, CE2A, CE1B, CE2B, REG, OE, WE, IORD, IOWR, WAIT, ACK, ADLE, DATDIR, DATOE.

I²C bus interface



The I²C bus timing characteristics and bus-line capacitance are given in below table, and below figure shows the timing definitions for the I²C bus. The minimum HIGH and LOW periods of the SCL clock specified in

below table determine the maximum bit transfer rates of 400kbits/sec for Fast-mode.

| Symbol | Item | Min | Max | Unit |
|--------------|--|-----|-----|-----------|
| f_{scl} | SCL frequency | | 400 | KHz |
| t_{BUF} | Bus free time between stop and start | 1.3 | | μ sec |
| $t_{HD,STA}$ | Hold time start condition | 0.3 | | μ sec |
| t_{LOW} | SCL low period | 1.3 | | μ sec |
| t_{HIGH} | SCL high period | 0.6 | | μ sec |
| $t_{SU,STA}$ | Setup time before a repeated start | 0.6 | | μ sec |
| $t_{HD,DAT}$ | Data hold time | 0 | 0.9 | μ sec |
| $t_{SU,DAT}$ | Data setup time | 100 | | nsec |
| t_R | Rise time for both SDA and SCL signals | 20 | 300 | nsec |
| t_F | Fall time for both SDA and SCL signals | 20 | 300 | nsec |
| $t_{SU,STO}$ | Setup time before a stop condition | 0.6 | | nsec |
| C_b | Capacitive load for each bus line | | 400 | pF |

6.2 Universal microprocessor Control Signal Generator (UCSG)

CICORE2.0 can be connected to various CPUs, which have a different external bus control structure, different signals, and different timings from one another. To interface with a large number of different microprocessors, the host microprocessor interface includes a fully configurable UCSG block that generates the right PCMCIA control signals.

Input control signals of a host microprocessor are CS, RD/DIR, WR/STR. Its output signals are WAIT/ACK and INT. Active levels of input and output can be selected by configuration bits, and the output buffer structure is also configurable as either open-drain or push-pull by the UCSG1 and UCSG2 registers.

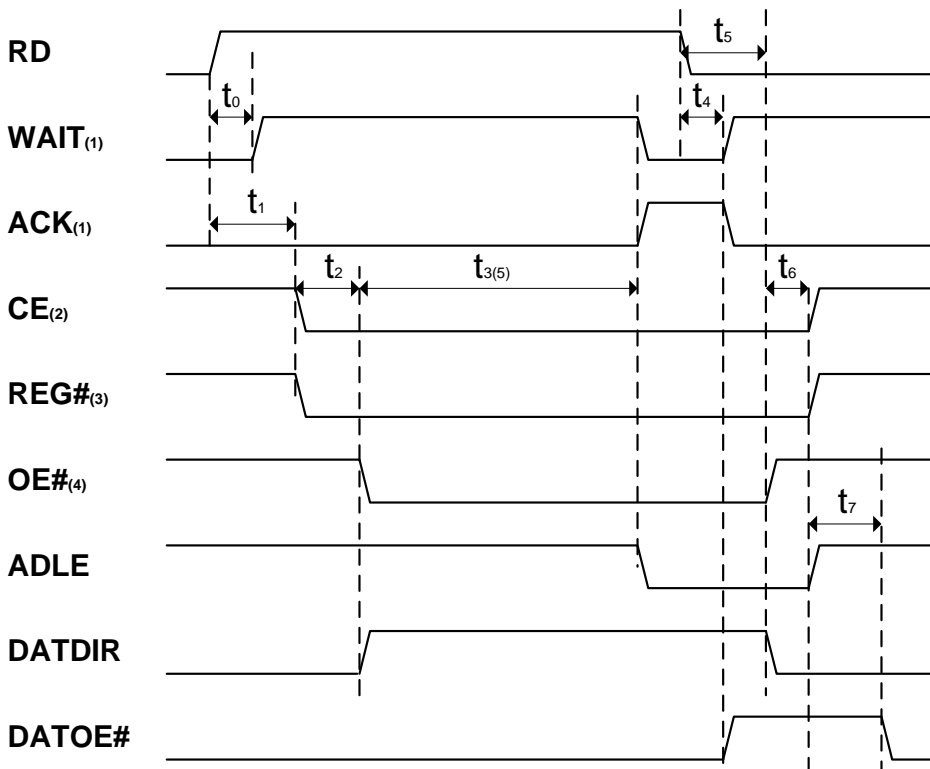
- CS(Chip Select): Chip select signal indicates to the CICORE2.0 that the current bus cycle is addressed to one of the modules (or external device)
- RD/DIR: Read strobe or direction signal. This signal function can be chosen with the RDIR bit. Read strobe indicates a valid read bus cycle. Direction signal indicates the bus transfer direction when a valid bus transfer is indicated by the transfer strobe signal
- WR/STR: Write strobe or transfer strobe. This signal function can be adjusted with the WSTR bit. Write strobe indicates a valid write bus cycle. or Transfer strobe indicates a valid bus transfer in direction indicated by RD/DIR state.

- **WAIT/ACK:** Wait or Acknowledge transfer. In WAIT mode, this signal inserts wait cycles in the bus read or write operation in process. In ACK mode, this signal indicates the completion of the bus cycle.
- **INT:** Interrupt output to the host microprocessor.

The UCSG (universal control signals generator) inputs the RD / DIR, WR / STR and CS signals from host microprocessor, WAITA# and WAITB# from the modules and generates all the control signals to modules, host microprocessor, buffers and external device: CE1A#, CE2A#, CE1B#, CE2B#, REG#, OE#, WE#, IORD#, IOWR#, WAIT, ACK, ADLE, ADOE#, DATDIR, and DATOE#.

The INT output to the microprocessor can be configured as active high or low and driven in the push-pull or the open-drain mode. Interrupts are controlled by CICORE2.0 and one output is used for connection of CICORE2.0 to the microprocessor interrupt controller. Five interrupt sources are available: two for modules detection, two for module IRQ, and one for external device. Modules detection interrupts are latched inside the CICORE2.0 and are acknowledged on the reading of the Interrupt Status Register. Each interrupt source can be individually masked. When masked, an incoming interrupt is visible in the Interrupt Status Register but does not generate an interrupt to the host microprocessor.

6.3 Read Access



Notes

- (1) The WAIT/ACK output is either WAIT or ACK signal formatted according to the WAIT/ACK pin settings (driving structure, active level)
- (2) There are three read access types. According to the read access type, CE(Chip Enable) signal is selected: either CE1A# or CE1B# for memory access, I/O to module A or B; either CE2A# or CE2B# for EC(Extended Channel) access; EXTCS for external device access in regenerate mode.
- (3) REG# signal is not asserted during a common memory or external memory access.
- (4) OE# signal is asserted during a memory access(attribute or common). It is replaced by IORD# during an IO read cycle, an EC read cycle, or a read cycle of an external device in regenerate mode.
- (5) t3 can be lengthened by the insertion of wait cycles. When the module asserts WAIT# signal, t3 cycle counter stops until WAIT# becomes inactive anew.

Memory read timings are given for various cycle durations. In attribute memory mode, only 600 nsec and 300 nsec cycles are available. In common memory mode, the 300 nsec cycle isn't available. IO and external devices in regenerate mode share the same timing specifications because all of them use IORD# and IOWR# signals. Timings are given in CICORE2.0 clock cycles. They are calculated to comply with PCMCIA specifications when 27 MHz clock is used.

*unit : ns(cycle)

| | Memory read | | | | | | IO, EC, EXT |
|--------|-------------|--------|--------|--------|--------|--------|----------------|
| | 600 | 300 | 250 | 200 | 150 | 100 | |
| t0 max | 15 | | | | | | |
| t1 max | 74(2) | | | | | | |
| t2 | 111(3) | 37(1) | 37(1) | 37(1) | 37(1) | 37(1) | 74(2) |
| t3 | 518(14) | 296(8) | 259(7) | 185(5) | 148(4) | 111(3) | 111(3) |
| t4 min | 15 | | | | | | |
| t5 max | 74(2) | | | | | | |
| t6 | 37(1) | | | | | | |
| t7 | 185(5) | 111(3) | 111(3) | 111(3) | 111(3) | 74(2) | 74(2) |

Notes

- t0: delay between start of a read cycle and activation of WAIT
- t1: delay between start of a read cycle and falling edge of CE and REG# (if required for the current cycle)
- t2: delay between falling edge of CE and falling edge of OE# (and switching of the data buffer direction control)

t3: delay between falling edge of OE# and falling edge of WAIT (and switching of the data buffer direction control)

t4: read cycle length. This delay is necessary for a module to place the read data on the data output bus. After t4 delay is expired, WAIT is deasserted and ACK asserted. Then the processor is enabled to read the data on the bus. At the same time, ADLE is reset to latch the address sent to the module so that the data is not changed while the processor is reading. t4 can be lengthened if the module requires extra wait cycles by asserting its WAIT# pin low.

t5: delay to deassertion of module read signal (OE# or IORD#) after minimum delay after t4.

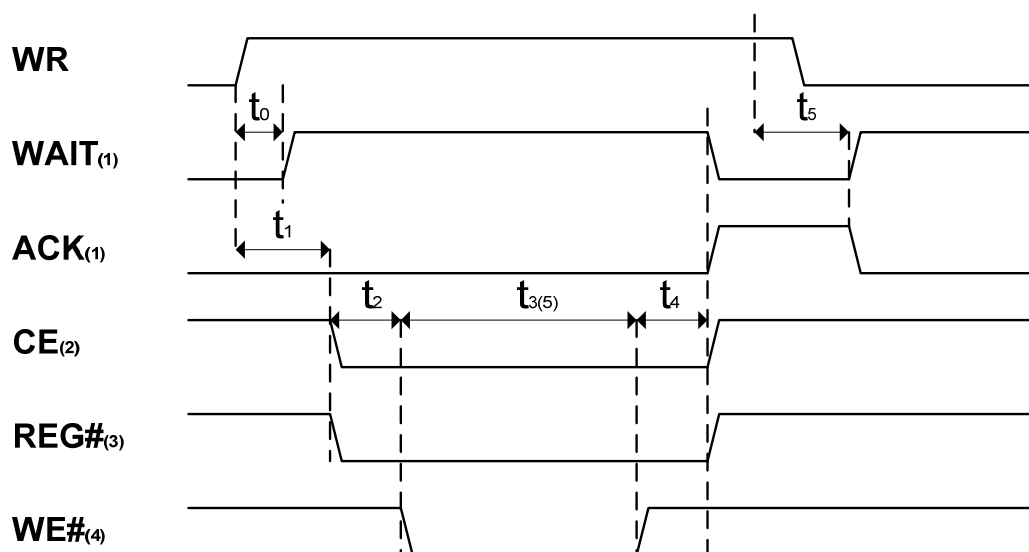
t6: delay between end of read cycle indicated by the processor and data bus isolation (DATOE# asserted)

t7: delay between data bus isolation and switching back of the data bus direction

t8: delay to deassertion of module read signal (OE# or IORD#) after end of a read cycle by the processor.

t7: delay between deassertion of the module read signal and re-enabling of the data bus (see t7 on write cycle)

6.4 Write Access



Notes

(1) The WAIT/ACK output is either WAIT or ACK signal formatted according to the WAIT/ACK pin settings (driving structure, active level)

(2) There are three write access types. According to the write access type, CE(Chip Enable) signal is selected: either CE1A# or CE1B# for memory access, I/O to module A or B; either CE2A# or CE2B# for EC(Extended Channel) access; EXTCS for external device access in regenerate mode.

(3) REG# signal is not asserted during a common memory or external access.

(4) WE# signal is asserted during a memory access(attribute or common). It is replaced by IOWR# during an IO write cycle, an EC write cycle, or an external device in regenerate mode.

(5) t3 can be lengthened by the insertion of wait cycles. When the module asserts WAIT# signal, t2 cycles counter stops until WAIT# becomes inactive anew.

Memory write timings are valid for both attribute and common memory mode. IO and external devices in regenerate mode share the same timing specifications because all of them use IORD# and IOWR# signals. Timings are given in CICORE2.0 clock cycles. They are calculated to comply with PCMCIA specifications when 27 MHz clock is used.

*unit: ns (cycle)

| | Memory write | | | | | IO, EC, EXT |
|--------|--------------|--------|--------|--------|-------|----------------|
| | 600 | 250 | 200 | 150 | 100 | |
| t0 max | 15 | | | | | |
| t1 max | 74(2) | | | | | |
| t2 | 74(2) | 37(2) | | | | 74(2) |
| t3 | 333(9) | 185(5) | 148(4) | 111(3) | 74(2) | 185(5) |
| t4 | 74(2) | 37(1) | | | | 37(1) |
| t5 max | 15 | | | | | |

Notes

t0: delay between start of a write cycle and activation of WAIT

t1: delay between start of a write cycle and assertion of CE and REG# (if necessary for the current cycle)

t2: delay to assertion of the write signal (WE# or IOWR#) after the assertion of CE

t3: write cycle duration. This delay can be lengthened by the assertion of the module WAIT# pin

t4: delay between deassertion of the write signal and deassertion of CE, REG# and WAIT and assertion of ACK indicating to the processor the end of its write cycle

t5: delay between end of the write cycle and deassertion of ACK

6.4 MPEG transport stream control

In normal mode operation, the 3rd transport stream is excluded and the rest is the same. The following notation is used in this document for easy explanation: 1st TSI, 2nd TSI, 1st TSO, 2nd TSO. 1st TSI and 2nd TSI are the input signals of MPEG transport stream interface block within CICORE2.0. 1st TSO and 2nd TSO are the output signals of MPEG transport stream interface block within CICORE2.0. 1st TSI is routed

internally to 1st TSO and 2nd TSI is routed to 2nd TSO. In single mode operation, the intermediate transport stream from A is routed to 2nd TSO for easier, rapider, and more accurate channel change.

Single Mode

In single mode operation, CICODE2.0 can select one among three MPEG transport streams as an input stream using TSI[1:0] bits of single mode TS(Transport Stream) control register. The selected stream is assigned to the 1st TSI. The 1st TSI is routed to several selective destinations: 1) Module A, 2) Module B, 3) Both Module A and Module B, 4) Direct connection to the 1st TSO by assigning some values to TSIEN and TSOEN bits in the module control register. CICODE2.0 can also assign the transport stream output to DEMUX by setting TSO bit of single mode TS control register. CICODE2.0 also send the intermediate MPEG transport stream from module A to the 2nd TSO. It is very useful to find active module when mode changes. When the TSO bit is cleared, 1st TSO and 2nd TSO are routed to transport stream output 1 and transport stream 2 of CICODE2.0, respectively. When the TSO bit is set, 1st TSO is routed to transport stream output 2 and 2nd TSO to another transport stream output.

The third MPEG Transport stream input is controlled by TSI field in the single mode TS control register.

Twin mode

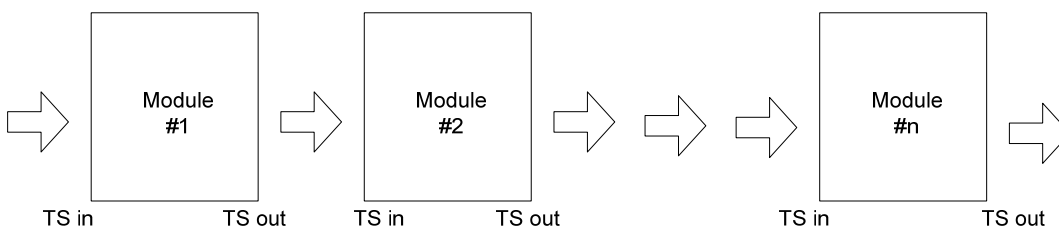
When a TWIN bit of twin mode TS control register is set, the mode is changed to twin mode. In twin mode operation, CICODE2.0 can select two among three MPEG transport stream as an input stream using MTSI[1:0] bits of twin mode TS control register. The selected stream is assigned to the 1st TSI and the 2nd TSI. They are routed to several selective destinations: 1) Module A, 2) Module B, 3) Both Module A and Module B, 4) Direct connection to the 1st TSO by assigning some values to TSIEN, TSOEN, and TSMAP bits in the module control register and twin mode TS(Transport Stream) control register. CICODE2.0 can also assign the transport stream output port to DEMUX by setting MTSO bit of twin mode TS control register. When the MTSO bit is cleared, the 1st TSO and the 2nd TSO are routed to transport stream output 1 and 2, respectively. When the MTSO bit is set, the 1st TSO is routed to transport stream output 2 and 2nd TSO is routed to transport stream output.

The third MPEG Transport stream input is controlled by MTS field in the Twin mode control register.

7. MPEG Transport Stream Transition

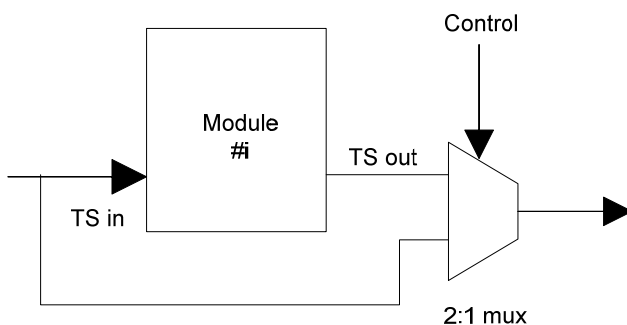
7.1 TS Daisy Chain

In the DVB Common Interface, each module has an MPEG input port and an MPEG output port composed of MPEG clock, MPEG packet start, MPEG valid data, MPEG data bus. The MPEG transport stream transits through the modules connected in a daisy chain basis.



7.2 Hot plug and bypass control

As a module can be inserted or removed at any time, the CICORE2.0 handles one MPEG transport stream bypass for each module. For this bypass, a valid DVB CI module is not recognized to be inserted and activated in the corresponding slot, and is recognized automatically without delay to be removed from a slot. The bypass is disabled by the TSOEN bit in each Module Control Register.

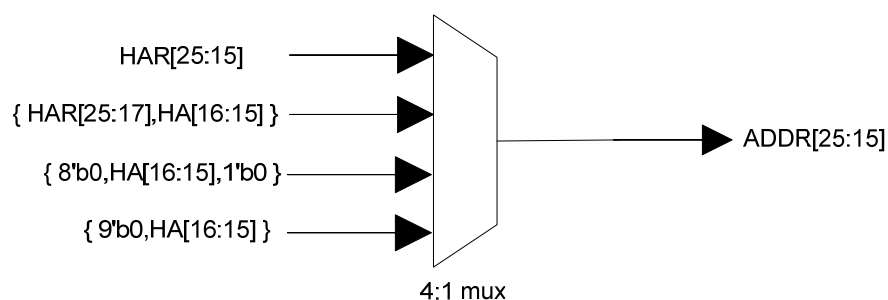


7.3 TS/Addresses input signals

In single mode operation, the selected MPEG transport stream is routed to among one of module A, module B, and both of the modules. It can bypass the modules by setting TSIEN and TSOEN bits of each Module

control register.

The MPEG input stream pins on the module are shared with the high address bits specified by the PC card standard. When a module is inserted, all these pins remain in the logic 0 level before initialization. If a memory module is recognized, the high address bits, ADDR[25:15] can be applied to the module by setting the HAD bit in the Module Control Register. The generation of ADDR[25:15] is controlled by HAM field in the ADDR generation control register.



If a DVB module is recognized, the MPEG stream is applied to the module by setting the TSIEN bit in the Module Control Register. Those two bits cannot be set at the same time and are cleared when the module is extracted. The TSOEN bit (TS bypass control bit) can only be set when TSIEN has previously been set. Clearing TSIEN also clears TSOEN.

In twin mode operation, the 1st TSI and the 2nd TSI are routed to several selective destinations: 1) Module A, 2) Module B, 3) Both Module A and Module B, 4) The 1st TSO or the 2nd TSO by assigning some values to TSIEN, TSOEN, TS1B, TS2B, and TSMAP bits in the module control register and the twin mode TS control register.

The effect of TSIEN and TSOEN bit is the same as single mode operation. When the TS1B, 1st TSI bypass enable, bit, is set, the 1st TSI is routed directly to 1st TSO and 2nd TSI is routed like single mode selected TS. When the TS2B, 2nd TSI bypass enable, bit, is set, the 2nd TSI is routed directly to 2nd TSO and 1st TSI is routed like single mode selected TS. When both of the TS1B and TS2B are cleared, then TSMAP bit is available. In this case, 1st TSI and 2nd TSI are mapped to each module according to the TSMAP bit. When the TSMAP bit is cleared, 1st TSI is routed to 1st TSO through module A and 2nd TSI is routed to 2nd TSO through module B. When the TSMAP bit is set, 1st TSI is routed to 1st TSO through module B and 2nd TSI is routed to 2nd TSO through module A.

In order to record one program and watch another program in one TS, it is possible to execute the two operations simultaneously with the TS.

CICORE2.0 supports ALL_TS1 and ALL_TS2 bits of single mode TS control register. In such case ALL_TS1 and ALL_TS2 bits are very useful. When ALL_TS1 bit is set, the selected 2nd TSI in MTSI[1:0] is replaced by 1st TSI. So the same TS(selected 1st TSI) is individually processed according to TS1B, TS2B and TSMAP bits of twin mode TS control register. When ALL_TS2 bit is set, the selected 1st TSI is replaced by 2nd TSI. So

the same TS(selected 2nd TSI) is individually processed. For recording some program, it is desirable to use twin mode.

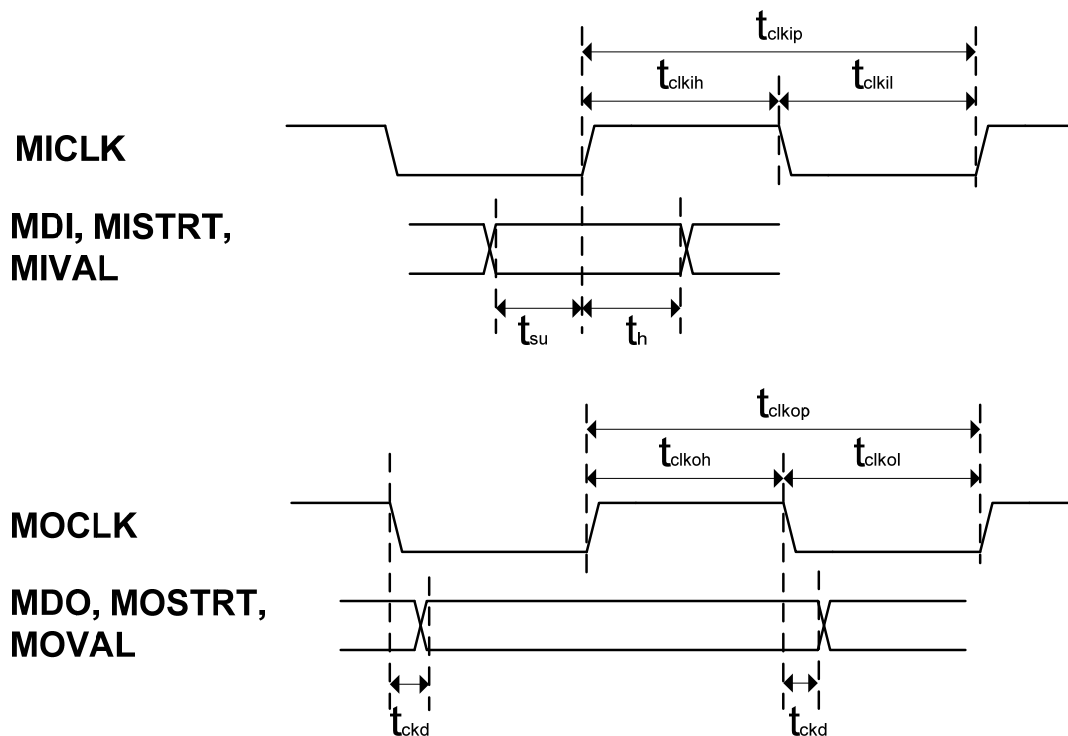
7.4 Invert Mask

Some modules can output an MPEG stream with inverted bits in the MPEG data bus. The CICORE2.0 is able to re-invert those bits to restore the correct data on the bus. This is achieved by setting the appropriate bits in the Invert Mask Register.

7.5 MPEG Signals

The MPEG inputs of the CICORE2.0 should be connected to the MPEG source of the host or from another CICORE2.0. MPEG signals coming from this source should satisfy the timing limits defined in the DVB standard. The MPEG outputs can be connected to any MPEG compliant destination or another CICORE2.0. MPEG output signals are guaranteed to meet the provided timing specifications.

7.6 TS Signals Timing



| Symbol | Item | MIN | MAX | Unit |
|--------|-----------------------------|-----|-----|------|
| tclkip | MPEG input clock period | 111 | | ns |
| tclkih | MICLK input clock high time | 40 | 97 | ns |
| tclkil | MICLK input clock low time | 40 | 97 | ns |
| tclkop | MPEG output clock period | 111 | | ns |
| tclkoh | output clock high time | 40 | 91 | ns |
| tclkol | output clock low time | 40 | 91 | ns |
| tsu | input data setup | 15 | | ns |
| th | input data hold | 10 | | ns |
| tckd | clock to data delay | 0 | 15 | ns |

7.7 Command interface signals

The command interface is directly issued from PC Card standard restricted to 8 bit data access and 15 bit addressing. The command interface of a CI module is described in detail in the PC Card standard and the restrictions applied to this standard for the command interface are described in the DVB CI standard.

The 15 address bits and 8 data bits of the CI modules are connected to the host microprocessor bus through tri-state buffers (type 373 and 245) controlled by the CICORE2.0 which outputs an output enable and a direction control signal for each buffer group.

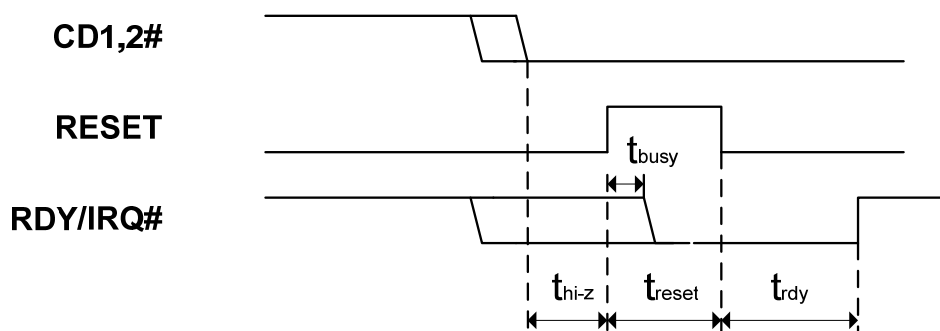
CICORE2.0 provides the buffers control signals. The buffers should be powered by the same source with the modules.

The CI control signals are the same with the PC Card control signals: CE1, CE2, REG, OE, WE, IORD, IOWR, RDY/IRQ, and WAIT. CICORE2.0 generates those signals that meet the PC Card standard whenever the host microprocessor accesses one of the modules.

The activated control signals depend on the access type chosen in the module control register with ACS[1:0]. The active level duration of read and write signals is configured by the memory access cycle time registers. CICORE2.0 receives RDY/IRQ from the module and retransmits the interruption to the host microprocessor. A module can also request WAIT. Then this internally generated WAIT period is added to the read/write duration to be transmitted to the host microprocessor.

7.8 Module Detection and Activation

After automatic detection of the insertion and removal of a module, the CICORE2.0 executes the programmed code every time. In order to detect a module, two pins on the connector: CD1# and CD2# must be simultaneously asserted to ensure that a module is inserted. When a module is inserted, the CICORE2.0 can automatically activate the module if programmed so when AUTO bit is asserted in the Module Control Register. The activation can also be handled manually by the host microprocessor by asserting the bits in the Module Control Register. The module activation consists in resetting the module and waiting for RDY signal to go high with respect to the PC card standard timings.



| Symbol | Item | Min | Max | Unit |
|-------------|---------------------------------|-----|-----|---------|
| t_{hi-z} | Card detect to reset driven | 300 | | ms |
| t_{reset} | Reset pulse width | 11 | | μ s |
| t_{busy} | Reset asserted to ready negated | | 10 | μ s |
| t_{rdy} | Reset negated to module ready | | 5 | s |

7.9 Interrupts

Interrupts are controlled by CICORE2.0. One interrupt output is available for connecting CICORE2.0 to the main microprocessor interrupt controller. Five interrupt sources are available: module detection IRQ and one external device interrupt are applied to the CICORE2.0 by using the external interrupt input pin. CICORE2.0 detects module detection interrupts internally. It is recognized by reading the Interrupt Status Register whether an interrupt occurs or not. Each interrupt source can be individually masked. When masked, an interrupt flag is stored in the Interrupt Status Register but an interrupt of the host microprocessor is not executed. The INT output to the host microprocessor can be configured as either active high or low and is driven by either a push-pull or an open drain.

7.10 Registers Description

CICORE2.0 includes several internal registers. All registers are reset to 00h. Register bits marked with X should not be set. They are read as 0.

| Register Address | Description |
|------------------|---|
| 00 | Module A Control Register |
| 01 | Module A auto select mask high Register |
| 02 | Module A auto select mask low Register |
| 03 | Module A auto select pattern high Register |
| 04 | Module A auto select pattern low Register |
| 05 | Memory access A cycle time Register |
| 06 | Invert Input Mask A Register |
| 07 | ADDR generation control Register |
| 08 | HA Register |
| 09 | Module B Control Register |
| 0A | Module B auto select mask high Register |
| 0B | Module B auto select mask low Register |
| 0C | Module B auto select pattern high Register |
| 0D | Module B auto select pattern low Register |
| 0E | Memory access B cycle time Register |
| 0F | Invert Input Mask B Register |
| 10 | Signal mode TS Control register |
| 11 | Twin mode TS Control Register |
| 12 | External access auto select mask high Register |
| 13 | External access auto select mask low Register |
| 14 | External access auto select pattern high Register |
| 15 | External access auto select pattern low Register |
| 16 | Reserved |
| 17 | Destination select Register |
| 18 | Power control Register |
| 19 | Reserved |
| 1A | Interrupt Status Register |
| 1B | Interrupt Mask Register |
| 1C | Interrupt Configure Register |
| 1D | Microprocessor Interface Configure Register |
| 1E | Microprocessor wait/ack Configure Register |
| 1F | CIMAX Control Register |

7.11 Registers Information

| Address | Description |
|---------|-------------|
|---------|-------------|

| | |
|-----------------------|---|
| <p>'h00 (h09)</p> | <p>Module A (Module B) control register</p> |
|-----------------------|---|

| | | | | | | | |
|-----|-------|-------|-----|------|------|------|-----|
| RST | TSOEN | TSIEN | HAD | ACS1 | ACS0 | AUTO | DET |
|-----|-------|-------|-----|------|------|------|-----|

- RST

RST pin control of common interface(CI) modules

Only able to be set when DET=1

Forced to 0 when DET=0

- TSOEN

MPEG transport stream bypass control

Only able to be set when DET=1, HAD=0, and TSIEN=1

Forced to 0 when DET=0 or TSIEN=0

0 : bypass enabled

1 : bypass disabled

- TSIEN

MPEG transport stream input control

Only able to be set when DET=1 and HAD=0

Forced to 0 when DET=0

0 : no MPEG stream

1 : MPEG stream enabled

- HAD

High order addresses in place of MPEG stream input

Only able to be set when DET=1, TSIEN=0, and TSOEN=0

Forced to 0 when DET=0

0 : apply MPEG stream

1 : apply A[25:15] for memory access

- ACS[1:0]

Module access type

Only able to be set when DET=1

Forced to "00" when DET=0

00 : access to attribute memory

01 : access to I/O space

10 : access to common memory

11 : access to Extended Channel using CE2# signal

- AUTO Module auto activation on detection
 - 0 : no auto activation procedure
 - 1 : start module auto activation when DET=1 and module power on

- DET Module detection
 - 0 : no module present
 - 1 : module inserted

'h01 Module A (Module B) auto select mask high register

('h0A)

| | | | | | | | |
|---|---|---|---|---|------|------|------|
| X | X | X | X | X | MA25 | MA24 | MA23 |
|---|---|---|---|---|------|------|------|

'h02 Module A (Module B) auto select mask low register

('h0B)

| | | | | | | | |
|------|------|------|------|------|------|------|------|
| MA22 | MA21 | MA20 | MA19 | MA18 | MA17 | MA16 | MA15 |
|------|------|------|------|------|------|------|------|

- MA[25:15] Address mask for decoding
 - 0 : the address bit doesn't care
 - 1 : the address bit should match the programmed address bit in module auto select pattern register

'h03 Module A (Module B, External) auto select pattern high register

('h0C,'h14)

| | | | | | | | |
|---|---|---|---|---|------|------|------|
| X | X | X | X | X | PA25 | PA24 | PA23 |
|---|---|---|---|---|------|------|------|

'h04 Module A (Module B, External) auto select pattern low register

('h0D,'h15)

| | | | | | | | |
|------|------|------|------|------|------|------|------|
| PA22 | PA21 | PA20 | PA19 | PA18 | PA17 | PA16 | PA15 |
|------|------|------|------|------|------|------|------|

- PA[25:15] Address pattern to match in accordance with address mask to select the corresponding module.
 - Relevant only when DEF=0 in external auto select mask. Don't care if DEF=1.

'h05 Module A (Module B) Memory access cycle time register

('h0E)

| | | | | | | | |
|---|-----|-----|-----|---|-----|-----|-----|
| X | AM2 | AM1 | AM0 | X | CM2 | CM1 | CM0 |
|---|-----|-----|-----|---|-----|-----|-----|

- AM[2:0] Attribute memory cycle time used

| | |
|-----|---------|
| 000 | : 100ns |
| 001 | : 150ns |
| 010 | : 200ns |
| 011 | : 250ns |
| 100 | : 600ns |

101 to 111 : reserved. Do not use

This timing is valid for write access. During read access, if AM=100, 600ns cycles will be used, and
if AM=0XX, 300ns will be used.

- CM[2:0] Common memory cycle time used

| | |
|-----|---------|
| 000 | : 100ns |
| 001 | : 150ns |
| 010 | : 200ns |
| 011 | : 250ns |
| 100 | : 600ns |

101 to 111 : reserved. Do not use

'h06 Module A (Module B) Invert input mask register

('h0F)

| | | | | | | | |
|------|------|------|------|------|------|------|------|
| INV7 | INV6 | INV5 | INV4 | INV3 | INV2 | INV1 | INV0 |
|------|------|------|------|------|------|------|------|

- INV[7:0] Invert mask
 - 0 : corresponding bit is not complemented
 - 1 : corresponding bit is complemented

'h07 ADDR generation control

| | | | | | | | |
|--------|--------|---|---|---|---------|---------|---------|
| HAM[1] | HAM[0] | X | X | X | HAR[25] | HAR[24] | HAR[23] |
|--------|--------|---|---|---|---------|---------|---------|

- HAM[1:0] 11: ADDR = HAR[25:15]
 10: ADDR = {HAR[25:17], HA[16:15]}
 01: ADDR = {8'b0, HA[16:15], 1'b0}
 00: ADDR = {9'b0, HA[16:15]}

- HAR[25:23] HA register is used to build ADDR.

'h08 HA Register

| | | | | | | | |
|---------|---------|---------|---------|---------|---------|---------|---------|
| HAR[22] | HAR[21] | HAR[20] | HAR[19] | HAR[18] | HAR[17] | HAR[16] | HAR[15] |
|---------|---------|---------|---------|---------|---------|---------|---------|

- HAR[22:15] HA register is used to build ADDR.

'h10 Signal mode TS Control register

| | | | | | | | |
|---|---|---------|---------|---|------|------|-----|
| X | X | ALL_TS1 | ALL_TS2 | X | TSI1 | TSI0 | TSO |
|---|---|---------|---------|---|------|------|-----|

- ALL_TS1 In twin mode, selected 2nd TSI replace control.
 Setting this bit, selected 2nd TSI is replaced by 1st TSI.
 Then selected same 1st TSI is processed individually in twin mode.
 Don't care in single mode. Setting this bit is allowed only in twin mode.
 0 : selected 2nd TSI is processed
 1 : selected 2nd TSI is replaced by 1st TSI

In twin mode, selected 1st TSI replace control.

- ALL_TS2 Setting this bit, selected 1st TSI is replaced by 2nd TSI.
 Then selected same 2nd TSI is processed individually in twin mode.
 Don't care in single mode. Setting this bit is allowed only in twin mode.
 0 : selected 1st TSI is processed
 1 : selected 1st TSI is replaced by 2nd TSI

- TSI[1:0] MPEG transport stream input select control
 Don't care in twin mode. Setting this bit is allowed only in single mode.
 00 : TSI1 input stream enable
 01 : TSI2 input stream enable

10 : TSI3 input stream enable

11 : RFU

- TSO MPEG transport stream output select control
Don't care in twin mode. Setting this bit is allowed only in single mode.
0 : TSO1 output stream enable (TSO2 output A module's output)
1 : TSO2 output stream enable (TSO1 output A module's output)

'h11 Twin mode TS Control register

| | | | | | | | |
|------|---|-------|------|------|-------|-------|------|
| TWIN | X | TSMAP | TS1B | TS2B | MTSI1 | MTSI0 | MTSO |
|------|---|-------|------|------|-------|-------|------|

- TWIN MPEG transport stream twin function enable control
0 : Twin function disable
1 : Twin function enable
- TSMAP MPEG transport stream module mapping control
Automatically forced to 0 when TWIN=0.
Setting this bit is only allowed when TWIN=1 and TS1B=0 and TS2B=0
0 : 1st TSI => A module => 1st TSO, 2nd TSI => B module => 2nd TSO
1 : 1st TSI => B module => 1st TSO, 2nd TSI => A module => 2nd TSO
- TS1B 1st MPEG transport input stream bypass control
Automatically forced to 0 when TWIN=0. Setting this bit is only allowed when TWIN=1
If this bit is set, 2nd TSI operate like single mode TSI
0 : 1st TSI bypass(routed 1st TSO directly) disable
1 : 1st TSI bypass(routed 1st TSO directly) enable
- TS2B 2nd MPEG transport input stream bypass control
Automatically forced to 0 when TWIN=0. Setting this bit is only allowed when TWIN=1
If this bit is set, 1st TSI operate like single mode TSI
0 : 2nd TSI bypass(routed 2nd TSO directly) disable
1 : 2nd TSI bypass(routed 2nd TSO directly) enable
- Multi MPEG transport stream input select control
MTSI[1:0]

Automatically forced to 0 when TWIN=0. Setting this bit is only allowed when TWIN=1

00 : TSI1 => 1st TSI, TSI2 => 2nd TSI

01 : TSI2 => 1st TSI, TSI1 => 2nd TSI

10 : TSI1 => 1st TSI, TSI3 => 2nd TSI

11 : TSI3 => 1st TSI, TSI2 => 2nd TSI

• MTSO

Multi MPEG transport stream output select control

Automatically forced to 0 when TWIN=0. Setting this bit is only allowed when TWIN=1

Internally 1st TSI is routed to 1st TSO and 2nd TSI to 2nd TSO

0 : 1st TSO => TSO1, 2nd TSO => TSO2

1 : 1st TSO => TSO2, 2nd TSO => TSO1

'h12 External access auto select mask high register

| | | | | | | | |
|-----|---|---|---|---|------|------|------|
| DEF | X | X | X | X | MA25 | MA24 | MA23 |
|-----|---|---|---|---|------|------|------|

'h13 External access auto select mask low register

| | | | | | | | |
|------|------|------|------|------|------|------|------|
| MA22 | MA21 | MA20 | MA19 | MA18 | MA17 | MA16 | MA15 |
|------|------|------|------|------|------|------|------|

• DEF

External device default addressing

0 : EXTCS asserted when address match mask and pattern

1 : EXTCS asserted when neither module A nor module B is selected while CS input active

• MA[25:15]

Address mask for decoding

Relevant only when DEF=0. Don't care if DEF=1.

0 : the address bit doesn't care

1 : the address bit should match the programmed address bit in module auto select pattern register

'h17 Destination select register

| | | | | | | | |
|---|---|--------|---------|--------|------|------|---------|
| X | X | XCSDRV | XCSSLVL | XCSMOD | SEL1 | SELO | AUTOSEL |
|---|---|--------|---------|--------|------|------|---------|

- XCSRDRV EXTCS output pin structure

Changing this bit is only allowed when LOCK=0

0 : EXTCS buffer is open-drain

1 : EXTCS buffer is push-pull

- XCSLVL EXTCS output pin active level

Changing this bit is only allowed when LOCK=0

0 : EXTCS pin is active-low

1 : EXTCS pin is active-high

- XCSEMOD EXTCS generation mode

Changing this bit is only allowed when LOCK=0

0 : transmit EXTCS

1 : Regenerate EXTCS (default)

- SEL[1:0] Module select

Relevant only when AUTOSEL=0

00 : no destination selected

01 : select module A

10 : select module B

11 : select external device using EXTCS

- AUTOSEL Automatic module selection

Uses high order addresses to choose module or external device (using EXTCS)

0 : manual selection

1 : automatic selection

'h18 Power control register

| | | | | | | | |
|-------|-------|---|-------|-------|-------|---|-------|
| VCDRV | VCLVL | X | VAUTO | VCCEB | VCCEA | X | VCCAE |
|-------|-------|---|-------|-------|-------|---|-------|

- VCDRV Module VCC output pin structure

Changing this bit is only allowed when LOCK=0

0 : VCC buffer is open-drain

1 : VCC buffer is push-pull

- VCLVL Module VCC output pin active level

Changing this bit is only allowed when LOCK=0

0 : VCC pin is active-low

1 : VCC pin is active-high

- VAUTO Automatic module power on by module detection

Changing this bit is only allowed when LOCK=1

0 : disable auto power-on

1 : enable auto power-on

- VCCEB Module power supply switch control for Module B

Changing this bit is only allowed when LOCK=1

0 : power off

1 : power on

- VCCEA Module power supply switch control for Module A

Module power supply switch control for both Module A and B

0 : power off

1 : power on

- VCCAE Module power control for both Module A and B

Changing this bit is only allowed when LOCK=1

0 : power off

1 : power on

'h1A Interrupt status register

| | | | | | | | |
|---|---|---|-----|------|------|------|------|
| X | X | X | EXT | IROB | IROA | DETB | DETA |
|---|---|---|-----|------|------|------|------|

- EXT EXTINT status

0 : EXTINT is inactive

1 : EXTINT is active

- IROB Slot B inverted IRQ line state

0 : IRQ on slot B is high(inactive)

1 : IRQ on slot B is low(active)

- IRQA Slot A inverted IRQ line state
0 : IRQ on slot A is high(inactive)
1 : IRQ on slot A is low(active)

- DETB Slot B module detection
Reset on read
0 : no change
1 : a module has been inserted or extracted in slot B

- DETA Slot A module detection
Reset on read
0 : no change
1 : a module has been inserted or extracted in slot A

'h1B Interrupt mask register

| | | | | | | | |
|---|---|---|------|-------|-------|-------|-------|
| 0 | 0 | 0 | EXTM | IROBM | IRQAM | DETBM | DETAM |
|---|---|---|------|-------|-------|-------|-------|

- EXTM External interrupt mask
0 : masked
1 : unmasked. An interrupt request from external source will be transmitted to the microprocessor
- IROBM Slot B IRQ mask
0 : masked
1 : unmasked. An interrupt request from module B will be transmitted to the microprocessor
- IRQAM Slot A IRQ mask
0 : masked
1 : unmasked. An interrupt request from module A will be transmitted to the microprocessor
- DETBM Slot B module detection mask

Reset on read

0 : masked

1 : unmasked. A module movement in slot B will generate an interrupt

• DETAM

Slot A module detection mask

0 : masked

1 : unmasked. A module movement in slot A will generate an interrupt

'h1C

Interrupt configure register

| | | | | | | | |
|---|---|---|---|---|-------|-------|--------|
| X | X | X | X | X | ITDRV | ITLVL | EXTLVL |
|---|---|---|---|---|-------|-------|--------|

• ITDRV

INT output pin structure

Changing this bit is only allowed when LOCK=0

0 : INT buffer is open-drain

1 : INT buffer is push-pull

• ITLVL

INT output pin active level

Changing this bit is only allowed when LOCK=0

0 : INT pin is active-low

1 : INT pin is active-high

• EXTLVL

EXTINT input pin active level

Changing this bit is only allowed when LOCK=0

0 : EXTINT pin is active-low

1 : EXTINT pin is active-high

'h1D

Microprocessor interface configuration register

| | | | | | | | |
|-------|-------|---|---|-------|---------|---------|------|
| ALLVL | DDLVL | X | X | CSLVL | WSTRLVL | RDIRLVL | RDIR |
|-------|-------|---|---|-------|---------|---------|------|

• ALLVL

ADLE active level

Changing this bit is only allowed when LOCK=0

0 : ADLE is active-high (default)

1 : ADLE is active-low

- DDLVL DATDIR active level

Changing this bit is only allowed when LOCK=0

0 : high for read (default)

1 : low for read

- CSLVL CS input active level

Changing this bit is only allowed when LOCK=0

0 : CS is active-low

1 : CS is active-high

- WSTRVLV WR/STR input active level

Changing this bit is only allowed when LOCK=0

0 : WR/STR is active-low

1 : WR/STR is active-high

- RDIRLVL RD/DIR input active level

Changing this bit is only allowed when LOCK=0

0 : RD is active-low. RD/DIR input is low during read transfer and high during write

1 : RD is active-high. RD/DIR input is high during read transfer and low during write

- RDIR RD/DIR and WR/STR inputs function

Changing this bit is only allowed when LOCK=0

0 : RD/WR mode

1 : DIR/STR mode

'h1E Microprocessor wait/ack configuration register

| | | | | | | | |
|---|---|---|---|---|------|------|------|
| X | X | X | X | X | WACK | WDRV | WLVL |
|---|---|---|---|---|------|------|------|

- WACK WAIT/ACK pin function

Changing this bit is only allowed when LOCK=0

0 : WAIT mode

1 : ACK mode

- WDRV WAIT/ACK output pin structure

Changing this bit is only allowed when LOCK=0

0 : WAIT/ACK buffer is open-drain

1 : WAIT/ACK buffer is push-pull

- WLVL WAIT/ACK output pin active level
Changing this bit is only allowed when LOCK=0
0 : WAIT/ACK pin is active-low
1 WAIT/ACK pin is active-high

'h1F CICORE2.0 control register

| | | | | | | | |
|-----|---|---|---|---|---|------|------|
| RST | X | X | X | 0 | 0 | EIAA | LOCK |
|-----|---|---|---|---|---|------|------|

- RST Reset chip
1 : reset
- EIAA Early Interrupt for Auto Activation
0 : Interrupt at the end of auto activation
1 : Interrupt at the start of auto activation
- LOCK Validates and locks the chip setup
0 : chip is not configured.
1 : chip is configured

8. Electrical Characteristics

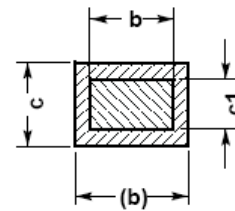
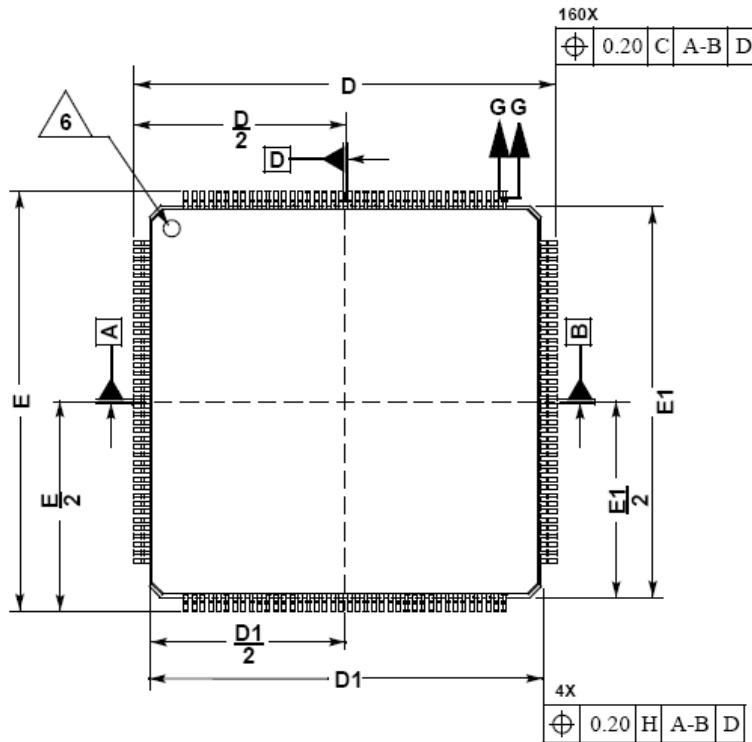
DC Characteristics

| Symbol | Parameter | Minimum | | Maximum | | Conditions | |
|-----------------|---------------------------|---------|------------------------|-----------------------|-----------------------|--------------------|--|
| | | TTL | CMOS | TTL | CMOS | V _{DD} | |
| V _{IL} | Input Low Level Voltage | -0.5V | -0.5V | 0.8V | 0.3xV _{DD} | 2.7V to 3.6V | Guaranteed Input Low Voltage |
| V _{IH} | Input High Level Voltage | 2.0V | 0.7xV _{DD} | V _{DD} +0.5V | V _{DD} +0.5V | 2.7V to 3.6V | Guaranteed Input High Voltage |
| V _{OL} | Output Low Level Voltage | | | 0.4V | 0.4V | 2.7V | I _{OL} = 1 to 6mA(CMOS) I _{OL} = 2 to 12mA(TTL) |
| V _{OH} | Output High Level Voltage | 2.4V | V _{DD} x 0.1V | | | 2.7V | I _{OH} = 1 to 6mA (CMOS) I _{OH} = 2 to 12mA (TTL) |

Recommended Operating Conditions

| Symbol | Parameter | Min | Max | Condition |
|--------|--------------------------|---------|----------|--------------------|
| | Power Supply | 2.7V | 3.6V | |
| VIL | Input Low Level Voltage | | | Guaranteed |
| | CMOS input | -0.5V | 0.2xVDD | Input Low Voltage |
| | TTL input | -0.5V | 0.8V | |
| VIH | Input High Level Voltage | | | Guaranteed |
| | CMOS input | 0.7xVDD | VDD+0.5V | Input High Voltage |
| | TTL input | 2.0V | VDD+0.5V | |
| | Junction Temperature | 0°C | 100°C | |

9. Package Dimension



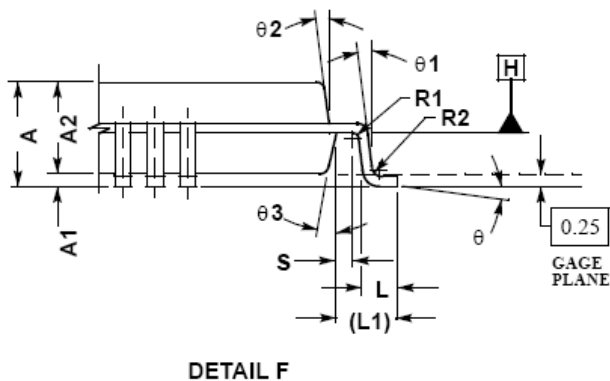
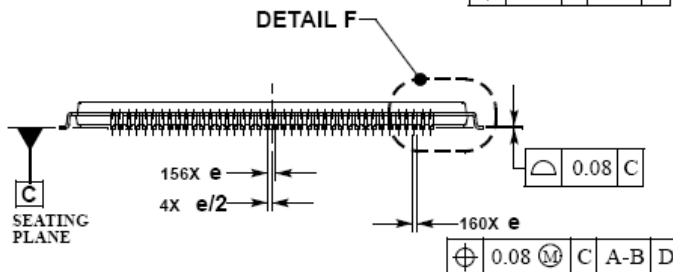
SECTION G-G

NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DATUMS A, B, AND D TO BE DETERMINED WHERE THE LEADS EXIT THE PLASTIC BODY AT DATUM PLANE H.
4. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PER SIDE. DIMENSIONS D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08mm. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN A PROTRUSION AND AN ADJACENT LEAD IS 0.07mm.



EXACT SHAPE OF CORNERS MAY VARY.



| DIM | MILLIMETERS | |
|---------|-------------|------|
| | MIN | MAX |
| A | --- | 1.60 |
| A1 | 0.05 | 0.15 |
| A2 | 1.35 | 1.45 |
| b | 0.17 | 0.27 |
| b1 | 0.17 | 0.23 |
| c | 0.09 | 0.20 |
| e1 | 0.09 | 0.16 |
| D | 26.00 BSC | |
| D1 | 24.00 BSC | |
| e | 0.50 BSC | |
| E | 26.00 BSC | |
| E1 | 24.00 BSC | |
| L | 0.45 | 0.75 |
| L1 | 1.00 REF | |
| R1 | 0.08 | --- |
| R2 | 0.08 | 0.20 |
| S | 0.20 | --- |
| theta | 0° | 7° |
| theta 1 | 0° | --- |
| theta 2 | 11° | 13° |
| theta 3 | 11° | 13° |